MALNAD COLLEGE OF ENGINEERING, HASSAN

(An Autonomous Institution Affiliated to VTU, Belagavi)

Autonomous Programme

Bachelor of Engineering

Department of
Electronics Engineering
(VLSI design & Technology)

SCHEME and SYLLABUS

(2025 Admitted Batch)

Academic Year 2026-27

VISION OF THE INSTITUTE

To be an institute of excellence in engineering education and research, producing socially responsible professionals.

MISSION OF THE INSTITUTE

1. Create conducive environment for learning and research
2. Establish industry and academia collaborations
3. Ensure professional and ethical values in all institutional endeavors

VISION OF THE DEPARTMENT

To build a dynamic center of excellence in VLSI and Semiconductor Technology education that empowers students to become innovative chip designers, technology leaders, and entrepreneurs driving advancements in semiconductor and intelligent electronic systems.

MISSION OF THE DEPARTMENT

1. To provide high-quality education in VLSI Design and Semiconductor Technology through a strong foundation in electronics engineering, modern laboratories, and industry-oriented learning.
2. To nurture innovation, creativity, and research skills by promoting project-based learning, internships, technical workshops, and collaboration with industry and research organizations.
3. To develop skilled and ethical professionals capable of designing advanced semiconductor and intelligent electronic systems for emerging

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Department of Electronics Engineering

(VLSI Design & Technology)

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO1: Design, develop, and test VLSI systems and semiconductor devices, and be successful professionals in VLSI and allied fields.

PEO2: Be effective leaders and team members with strong communication skills, professional ethics, and social responsibility.

PEO3: Possess the capability to pursue higher education and research in VLSI and allied domains and be lifelong learners.

PROGRAM OUTCOMES (POs)

1. **Engineering knowledge:** Apply knowledge of mathematics, natural science, computing, engineering fundamentals and an engineering specialization as specified in WK1 to WK4 respectively to develop to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions with consideration for sustainable development. (WK1 to WK4)
3. **Design/Development of solutions:** Design creative solutions for complex engineering problems and design/develop systems/components/processes to meet identified needs with consideration for public health and safety, whole-life cost, net zero carbon, culture, society and environment as required. (WK5)
4. **Conduct investigations of complex problems:** Conduct investigations of complex engineering problems using research-based knowledge including design of experiments, modelling, analysis & interpretation of data to provide valid conclusions. (WK8).
5. **Engineering tool usage:** Create, select and apply appropriate techniques, resources and modern engineering & IT tools, including prediction and modelling recognizing their limitations to solve complex engineering problems. (WK2 and WK6)
6. **Engineer and the world:** Analyze and evaluate societal and environmental aspects while solving complex engineering problems for its impact on sustainability with reference to economy, health, safety, legal framework, culture and environment. (WK1, WK5, and WK7).

PROGRAM OUTCOMES (POs)

7. **Ethics**: Apply ethical principles and commit to professional ethics, human values, diversity and inclusion; adhere to national & international laws. (WK9)

8. **Individual and collaborative team work**: Function effectively as an individual, and as a member or leader in diverse/multi-disciplinary settings.

9. **Communication**: Communicate effectively and inclusively within the community and society at large, such as being able to comprehend and write effective reports and design documentation, making effective presentations considering cultural, language, and learning differences.

10. **Project management and finance**: Apply knowledge and understanding of engineering management principles and economic decision-making and apply these to one's own work, as a member and leader in a team, and to manage projects and in multidisciplinary environments.

11. **Life-long learning**: Recognize the need for and have the preparation and ability for i) independent and life-long learning ii) adaptability to new and emerging technologies and iii) critical thinking in the broadest context of technological change. (WK8)

PROGRAM SPECIFIC OUTCOMES

PSO1: Apply the fundamentals of VLSI Design, Semiconductor Technology, and Embedded Systems to design and develop efficient, reliable, and innovative integrated circuit solutions for real-world and industrial applications.

PSO2: Develop efficient ASIC/FPGA-based solutions for real-world applications in embedded systems, Artificial Intelligence (AI), Internet of Things (IoT), communication, and semiconductor industries with professional and ethical responsibility.

Scheme of Evaluation (Theory Courses)

Assessment	Marks
CIE 1 – conducted for 50 marks and reduced to 15 marks	**15**
CIE 2 – conducted for 50 marks and reduced to 15 marks	**15**
Activities as decided by course faculty	**20**
SEE	**50**
Total	**100**

Scheme of Evaluation (Laboratory Courses)

Assessment	Marks
Continuous Evaluation in every lab session by the Course Coordinator	**10**
Record Writing	**20**
Laboratory CIE conducted by the Course Coordinator	**20**
SEE	**50**
Total	**100**

Examination	Maximum Marks	Minimum marks to qualify
CIE	50	20 (12+8)
SEE	50	20

COURSE TYPES

Basic Science Course	BSC
Applied Science Course	ASC
Engineering Science Course	ESC
Emerging Technology Course	ETC
Programming Language Course	PLC
Professional Core Course	PCC
Integrated Professional Core Course	IPCC
Professional Core Course Laboratory	PCCL
Professional Elective Course	PEC
Open Elective Course	OEC
Project/Mini Project/Internship	PI
Humanities and Social Sciences, Management Course	HSMC
Ability Enhancement Course	AEC
Skill Enhancement Course	SEC
Skill Development Course	SDC
Universal Human Value Course	UHV
Non-credit Mandatory Course	MC

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	THIRD SEMESTER										
Sl. No	**Course Category**	**Course Code**	**Course Title**	**Teaching & Learning Scheme**					**Exam Marks**			**Credits**
				L	**T**	**P**	**TW & SL**	**TH/S**	**CIE**	**SEE**	**Total**	
1	ASC/PCC	25VL301	Mathematics for VLSI	42	0	0	48	90	50	50	100	3
2	IPCC	25VL302	Analog Electronics-I	42	0	28	50	120	50	50	100	4
3	PCC	25VL303	Digital Electronics	42	0	0	48	90	50	50	100	3
4	PCC	25VL304	Digital system design using Verilog	42	0	0	48	90	50	50	100	3
5	PCC	25VL305	Physics of semiconductor devices	42	0	0	48	90	50	50	100	3
6	PCCL	25VL306	Digital system design using Verilog Lab	0	0	28	2	30	50	50	100	1
7	AEC	25VL307X	Ability Enhancement Course Laboratory **	0	0	28	2	30	50	50	100	1
8	SDC	25SCR	Community Project (Project-Based Learning)/ Societal Project	0	0	0	30	30	50	50	100	1
9	AEC	25PT1	Placement Training I	14	0	0	16	30	100	-	100	A
10	NCMC	25NYP1	NSS, YOGA, PE	0	0	0	28	28	100	-	100	A
11	NCMC	25BCM301	Bridge Mathematics-I (Non-Credit Mandatory Audit Course for Diploma entry students)	14	0	0	14	28	100	-	100	A
Total												19

Ability Enhancement Course (Laboratory)	
Course Code	**Course Name**
25VL307A	Linux Programming Laboratory
25VL307B	Programmable Logic Controllers
25VL307C	Simulation of Circuits and Devices
25VL307D	Numerical Computing Laboratory using GNU Octave / Scilab
TW & SL – Term Work and Self Learning, TH/S - Total Hours per Semester	

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	FOURTH SEMESTER										
Sl. No	**Course Category**	**Course Code**	**Course Title**	**Teaching & Learning Scheme**					**Exam Marks**			**Credits**
				L	**T**	**P**	**TW & SL**	**TH/S**	**CIE**	**SEE**	**Total**	
1	ASC/PCC	25VL401	Programmable Logic Devices and FPGA	42	0	0	48	90	50	50	100	3
2	IPCC	25VL402	Analog Electronics-II	42	0	28	50	120	50	50	100	4
3	PCC	25VL403	Network Analysis	42	0	0	48	90	50	50	100	3
4	PCC	25VL404	Computer Organization and ARM Processor	42	0	0	48	90	50	50	100	3
5	PCC	25VL405	Control Systems	42	0	0	48	90	50	50	100	3
6	PCCL	25VL406	FPGA System Design Lab	0	0	28	2	30	50	50	100	1
7	AEC	25VL407X	Ability Enhancement Course Laboratory **	0	0	28	2	30	50	50	100	1
8	BSC		Biology for Engineers	14	0	0	16	30	50	50	100	1
9	SDC	25EVS	Environmental Science Project	0	0	0	30	30	50	50	100	1
10	AEC	25PT2	Placement Training II	14	0	0	16	30	100	-	100	A
11	NCMC	25NYP1	NSS, YOGA, PE	0	0	0	28	28	100	-	100	A
12	NCMC	25BCM301	Bridge Mathematics-I (Non-Credit Mandatory Audit Course for Diploma Entry students)	14	0	0	14	28	100	-	100	A
Total												20

Ability Enhancement Course (Laboratory)	
Course Code	**Course Name**
25VL407A	SPICE Programming for Electronic Circuits
25VL407B	Power Electronics
25VL407C	Data structures using python
25VL407D	Python for Measurement & Data Analysis

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	FIFTH SEMESTER										
Sl. No	**Course Category**	**Course Code**	**Course Title**	**Teaching & Learning Scheme**					**Exam Marks**			**Credits**
				L	**T**	**P**	**TW & SL**	**TH/S**	**CIE**	**SEE**	**Total**	
1	HSMC	25VL501	Technological Innovation and Management Entrepreneurship	42	0	0	48	90	50	50	100	3
2	IPCC	25VL502	Verification using System Verilog & UVM	42	0	28	50	120	50	50	100	4
3	PCC	25VL503	CMOS Digital VLSI Design	42	0	0	48	90	50	50	100	3
4	PCC	25VL504	Static Timing Analysis	42	0	0	48	90	50	50	100	3
5	PCCL	25VL505	Analog VLSI Lab	00	0	28	02	30	50	50	100	1
6	PEC	25VL55X	Professional Elective Course - I	42	0	0	48	90	50	50	100	3
7	BSC	25RMIP	Research Methodology and IPR	42	0	0	48	90	50	50	100	3
8	AEC	25PT3	Placement Training III	14	0	0	16	30	50	50	100	1
9	SDC	25HBP	Hackathon-Based Project	0	0	0	30	30	50	50	100	1
Total												22

Professional Elective Course I	
Course Code	**Course Name**
25VL551	Computer Architecture using RISC-V
25VL552	Internet of Things
25VL553	Art of Analog Layout
25VL554	Python for Semiconductor Design

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	SIXTH SEMESTER										
Sl. No	**Course Category**	**Course Code**	**Course Title**	**Teaching & Learning Scheme**					**Exam Marks**			**Credits**
				L	**T**	**P**	**TW & SL**	**TH/S**	**CIE**	**SEE**	**Total**	
1	IPCC	25VL601	Analog and Mixed Signal IC Design	42	0	28	50	120	50	50	100	4
2	PCC	25VL602	Design for Test	42	0	0	48	90	50	50	100	3
3	PCC	25VL603	VLSI Physical Design	42	0	0	48	90	50	50	100	3
4	PCCL	25VL604	Analog and Mixed Signal Lab	00	0	28	02	30	50	50	100	1
5	PEC	25VL66X	Professional Elective Course - II	42	0	0	48	90	50	50	100	3
6	OEC		Open Elective Course - I	42	0	0	48	90	50	50	100	3
7	AEC	25PT4	Placement Training IV	14	0	0	16	30	50	50	100	1
8	NCMC	25UHV	Universal Human Values (VTU Online Course)	14	0	0	16	30	100	-	100	A
9	PI	25PRJ1	Capstone Project – Phase I	00	0	0	90	90	50	50	100	3
Total												21

Professional Elective Course II	
Course Code	**Course Name**
25VL661	Neuromorphic Computing
25VL662	VLSI Data Conversion Circuits
25VL663	Memory Design
25VL664	Hardware Security

Open Elective Course I	
Course Code	**Course Name**
25OEVL61	Digital System Design using Verilog
25OEVL62	PCB Design
25OEVL63	Consumer Electronics
25OEVL64	Basic VLSI Design

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	SEVENTH SEMESTER										
Sl. No	**Course Category**	**Course Code**	**Course Title**	**Teaching & Learning Scheme**					**Exam Marks**			**Credits**
				L	**T**	**P**	**TW & SL**	**TH/S**	**CIE**	**SEE**	**Total**	
1	IPCC	25VL701	System on Chip (SoC)	42	0	28	50	120	50	50	100	4
2	PCC	25VL702	Application-Specific Integrated Circuits	42	0	0	48	90	50	50	100	3
3	PCC	25VL703	Low Power IC Design	42	0	0	48	90	50	50	100	3
4	PEC	25VL77X	Professional Elective Course - III	42	0	0	48	90	50	50	100	3
5	OEC	25VL78X	Professional Elective Course - IV	42	0	0	48	90	50	50	100	3
6	PI	25PRJ2	Capstone Project – Phase II	0	0	0	210	210	100	100	200	7
7	NCMC	25IKS	Indian Knowledge System (VTU Online Course)	14	0	0	16	30	100	-	100	A
Total												23

Professional Elective Course - III	
Course Code	**Course Name**
25VL771	High-Speed PCB Design
25VL772	AI Hardware and Machine Learning
25VL773	Power Management Techniques for Integrated Circuit Design
25VL774	Micro-fabrication and Mems

Professional Elective Course - IV	
Course Code	**Course Name**
25VL781	VLSI Processor Design
25VL782	Scripting Languages for VLSI Design Automation
25VL783	RF Circuit Design
25VL784	Advanced Semiconductor Devices

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	EIGHTH SEMESTER										
Sl. No	**Course Category**	**Course Code**	**Course Title**	**Teaching & Learning Scheme**					**Exam Marks**			**Credits**
				L	**T**	**P**	**TW & SL**	**TH/S**	**CIE**	**SEE**	**Total**	
1	PEC	25SW01	Professional Elective Course - V (NPTEL Online Course)	0	0	0	90	90	50	50	100	3
2	OEC	25SW02	Open Elective Course - II (NPTEL Online course)	0	0	0	90	90	50	50	100	3
3	PI	25INT	Internship (15 weeks)	-	-	-	-	360	100	100	200	9
Total								**540**	**200**	**200**	**400**	**15**

Community/Societal Project

A community is a social unit or group of people sharing socially significant characteristics, such as place, set of norms, culture, religion, values, customs or identity. A community project involves addressing issues or needs within such a community or a network of entities working towards a common purpose. These projects may cover a wide range of areas, including welfare, sustainability, technology integration, and social development. Examples include establishing and maintaining an orphanage, implementing solar power generation and its maintenance, or developing environmental improvement solutions, etc. A community project is an experiential learning activity that encourages students to identify, analyze, and address real-life problems of the community using engineering knowledge. It aims to promote social responsibility and civic engagement, interdisciplinary thinking and collaboration and practical application of theoretical concepts, thereby enabling students to contribute meaningfully to community welfare and sustainable development. Students can take up projects individually or in a group not exceeding 4 students.

Environmental Science Project

The Environmental Science Project is an applied learning component designed to develop students' awareness, understanding, and responsibility toward the environment. It provides an opportunity to study real-world environmental issues and apply scientific and engineering principles to design feasible and sustainable solutions. The topics under environment include, but not limited to, climate change, biodiversity, air and water pollution, land use, excess use of natural resources, earthquakes, rise in the earth's temperature, power generation, soil erosion, environment issues related programmme, etc. The project involves problem identification, field surveys, case studies, data collection, environmental audits, analysis, and proposal of remedial or preventive measures aimed at improving biodiversity, air quality, and thermal comfort, etc. Students can take up projects individually or in a group not exceeding 4 students. Students can opt for Interdisciplinary Project based on their interest.

Hackathon Based Project

The term hackathon is derived from the combination of hack (referring to clever problem-solving, not illegal activity) and marathon, which denotes an arduous (i.e., difficult) intellectual task requiring sustained effort, endurance, and mental resilience. The meaning of a hackathon varies depending on the specific context and intent. In an academic context, a hackathon can be considered to involve several concepts, ranging from resourceful, unconventional approaches to problem-solving. Though a hackathon is an event, typically lasting for a few days to address a specific challenge, for academic purposes, it is conducted as a noncompetitive semester-long activity. The evaluation is done as and when the project is completed, by a panel of industry experts. The hackathons not only help participants develop skills like problem-solving, critical thinking, creativity, teamwork, communication and time management, but also foster indigenous technology development, promote innovation and entrepreneurship, and contribute to non-formal learning and skill enhancement. Students can take up a hackathon project individually or in a group of not exceeding 4 students.

The respective BoS will announce the problem statements in the beginning of the 5th semester. The topic selected can be discipline specific, interdepartmental, industrial, social (refers to immediate human relations, interactions, and individual behavior within a community), societal (describes larger, general issues, institutions, and structures that define society as a whole), environmental, health, financial, or innovative in nature, leading to development of a working prototype, application, or product. Hackathon projects are aligned with the principles of Outcome-Based Education (OBE) and support the objectives of innovation, skill development, and experiential learning in engineering education. Projects shall be evaluated by industry experts, based on creativity, problem-solving approach, teamwork, and possible implementation, as far as possible, as and when the project is completed.

Capstone Project

The Capstone project is a comprehensive, year-long project carried out in two phases during 6th and 7th semesters of the undergraduate engineering/technology program. It integrates knowledge and skills acquired from multiple courses and disciplines to address a complex, real-world problem. This project provides students with an opportunity to apply scientific principles, engineering methodologies, and technological tools to conceive, design, implement and evaluate an engineering solution. It serves as a culminating academic experience to demonstrate program outcomes, including problem-solving ability, teamwork, communication skills, and practical application of engineering principles. Students can take up projects individually or in a group not exceeding 4 students. The group may have students from the same discipline and drawn from different disciplines.

Types of Capstone Projects: Capstone projects undertaken for one year may fall into one or more of the following categories:

a) Research-Oriented Projects

- Focus on investigating new concepts, theories, or technologies.
- aim to generate new knowledge or contribute to academic research.

b) Experimental/Analytical Projects

- Based on laboratory or field experiments to validate a hypothesis or study a phenomenon.
- Including detailed data collection, analysis, and interpretation.

c) Simulation/Modelling Projects

- Use computational tools to model, simulate, and predict system behavior.
- Reduce the need for physical prototyping in the initial stages.

d) Industrial/Industry-Sponsored Projects

- Carried out in collaboration with an industry partner, address real-world engineering problems faced by the organization.

e) Interdisciplinary/Multidisciplinary Projects

- Combine knowledge and techniques from multiple engineering domains or other fields such as management, medicine, or environmental sciences.

f) Entrepreneurial/Innovation Projects

- Focus on product or service innovation with potential for commercialization.
- Include aspects of market analysis, cost estimation, and business planning.

Course Title	Mathematics for VLSI		
Course Code	25VL301	(L-T-P) C	(3-0-0)3
Exam	3 hours	Hours/Week	3 hours
SEE	50 marks	Total Hours	42L + 48ABL = 90

Course Objective: To develop a strong foundation in signal analysis, Fourier series, Fourier transforms, Z-transforms, and optimization techniques essential for engineering applications. The course enables students to analyze continuous and discrete signals and apply mathematical tools for modeling, system analysis, and optimization problems relevant to VLSI and related engineering domains.

Course Outcomes (COs): Upon completion of the course, students shall be able to:

CO's	Course Outcomes	Mapping to POs	Mapping to PSOs
1.	Apply the fundamentals of signals, mathematical operations, and Fourier series to analyze engineering problems.	1, 2, 3, 5	1
2.	Analyze continuous and discrete-time signals using Fourier transforms, DFT, and FFT techniques.	1, 2, 3, 4, 5	1
3.	Apply Z-transform techniques to solve discrete-time system and signal analysis problems.	1, 2, 3, 4, 5	1
4.	Apply linear programming and optimization techniques to solve transportation and related engineering optimization problems.	1, 2, 3, 4, 5, 11	1

Course Contents:

Module1	11 Hours

Mathematical Introduction to Signals in VLSI Engineering: Introduction to Signals, Classification of Signals, Elementary Signals and Basic Operations on signals, Mathematical Analysis and Derivations and related problems.

Fourier Series: Periodic functions, Euler's formula, Dirichlet's condition, Fourier series of functions - Even and odd functions. Practical harmonic analysis.

Self-Study: Half rang Fourier series.

Module2	10 Hours

Fourier Transforms: Infinite Fourier transform, Infinite Fourier sine and cosine transforms, Properties-Linear property, change of scale, shifting property. Inverse transforms, Convolution theorem and its significance, Discrete Fourier transform (DFT), Fast Fourier transform (FFT).

Self-Study: Fourier transform of derivatives and integrals

Module3	10 Hours

Z-transform: Z-transform of Standard functions, Linearity property, damping rule, Shifting property, Initial and final value theorems.

Inverse Z-transform- Power series method, Partial fraction method.

Self-study: Inverse integral method

MODULE-4	11Hrs.

Optimization techniques: Introduction to optimization techniques, nature and characteristics of operation research. Introduction to Linear programming, graphical solution, solution by simplex and Big M Method.

Transportation problems: Introduction, Initial Basic feasible solution by North-West corner method, least cost method, Vogel's approximation method.

Self-study: Formulation of assignment problems, Hungarian Method-Problems

Note: Theorems and properties without proof applicable to all the modules.
Self-study is not included in SEE

Prescribed Textbooks:

Sl. No.	Book Title	Authors	Edition	Publisher	Year
1.	Linear Algebra and its Applications	David C. Lay, Steven R Layand J.J. McDonald	5	Pearson Education Ltd	2015

Reference Books:

Sl. No	Book Title	Authors	Edition	Publisher	Year
1.	Advanced Engineering Mathematics	E.Kreyszig	10	Wiley	2015
2.	Operations Research: An Introduction, Pearson Education.	Hamdy A. Taha,	4	Cenage publications	2014

eBooks and online course materials:

- https://www.geneseo.edu/~aguilar/public/assets/courses/233/main_notes.pdf

Online Courses and Video Lectures:

1. https://www.coursera.org/learn/introduction-to-linear-algebra
2. https://www.coursera.org/specializations/linear-algebra-elementary-to-advanced
3. NPTEL Courses on Engineering Mathematics
4. MIT Open Course Ware Mathematics
5. SWAYAM Online Courses

Teaching-Learning–Evaluation Scheme:

Sl. No	Teaching and Learning Method	No. of Hours/ Week	No. of Weeks	Hours/ Semester
1	Classroom Teaching & Learning	3	14	42
3	Student Study Hours –Self Learning	1	14	14
4	Activity Based Learning (ABL1&ABL2)	-	-	27
5	Evaluation of Learning Process	-	-	07
Total Hours				90

Proposed Assessment Plan:

Tool	Remarks	Marks
CIE	Two CIEs conducted for 50 marks each and reduced to 15marks	30
Assignment Details	Assignment 1 Assignment 2	20
Total		**50**

Activity Based Learning(27Hours)

ABL1(14Hours): Assignment 1 details		**Hours**
Writing Assignment with Problems on concerned to real world applications.	Submission of the final assignment report and evaluation. (Questions of Blooms level L3 and Higher)	14
Total		**14**
ABL2(13Hours): Assignment 2 details		
Problem Solving Assignment	Understand the input data requirements	1
	Formulate the methodology	4
	Design the solution	4
	Solving the problem and submission	4
Total		**13**

Evaluation of Learning Process(7Hours)

Type of Evaluation	**Hours**
CIE (1 and 2)	3
Assignment	1
Semester End Exam	3
Total	**7**

Course Articulation Matrix

Course Outcomes	Program Outcomes												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**
CO1	3	2	2	-	2	-	-	-	-	-	-	2	-
CO2	3	3	2	1	2	-	-	-	-	-	-	2	-
CO3	3	3	2	2	2	-	-	-	-	-	-	2	-
CO4	3	3	2	2	2	-	-	-	-	-	1	2	-

Course Title	ANALOG ELECTRONICS-I		
Course Code	25VL302	(L-T-P) C	(3-0-2)4
Exam	3 hours	Hours/Week	5 hours
SEE	50 marks	Total Hours	42L+28P+50ABL=120

Course Objective: To provide students with a comprehensive understanding of analog electronic circuits, including BJT and MOSFET amplifiers, feedback amplifiers, oscillators, power amplifiers, and current source circuits. The course enables students to analyze, design, and evaluate analog circuits used in electronic and VLSI applications.

Course outcomes: Upon completion of the course, the student shall be able to:

CO's	Course Outcomes	Mapping to POs	Mapping to PSOs
1.	Describe the operating principles, characteristics, and small-signal models of BJT and MOSFET amplifier circuits.	1, 2	1
2.	Analyze BJT and MOSFET amplifier circuits, feedback amplifiers, oscillators, and power amplifiers using appropriate circuit analysis techniques.	1, 2, 3, 4, 5, 8, 9	1
3.	Design and evaluate analog electronic circuits, including multistage amplifiers, feedback circuits, oscillators, and power amplifiers to meet specified performance requirements.	1, 2, 3, 4, 5, 8	1
4.	Analyze the operation and performance of current sources and current mirror circuits used in analog integrated circuits and VLSI applications.	1, 2, 3, 4, 5, 8, 9, 11	1

Course Contents:

Module1 — **11 Hours**

BJT Small-Signal Amplifiers: Base-biased amplifier, emitter-biased amplifier, small-signal operation, AC beta, AC resistance of the emitter diode, two-transistor model, analysis of BJT amplifiers.

Voltage Amplifiers: Voltage gain, multistage amplifiers.

CC and CB Amplifiers: Common-collector (CC) amplifier, output impedance, cascading CE and CC amplifiers, Darlington connection, voltage regulation, common-base (CB) amplifier.

Module2 — **10 Hours**

MOSFET Small-Signal Amplifiers: DC bias point, small-signal operation, signal current in drain, transconductance, voltage gain, small-signal equivalent circuit models, T-equivalent circuit model.

MOSFET Amplifier Configurations: Common-source amplifier (with and without source resistance), common-gate amplifier, source follower.

Module3 — **10 Hours**

Feedback Amplifiers: Principles of negative feedback, four types of negative feedback, VCVS, ICVS, VCIS, and ICIS amplifiers (no mathematical derivations).

Oscillators: Conditions for sinusoidal oscillation, Wien bridge oscillator, RC phase-shift oscillator, Colpitts oscillator, Hartley oscillator, crystal oscillator.

Power Amplifiers: Amplifier terms, load lines, Class A, Class B, Class B push-pull emitter follower, and Class C power amplifiers.

MODULE-4 — **11 Hours**

Current Sources and Current Mirrors: Ideal and practical current sources, BJT and MOSFET constant current sources, current source and current sink configurations, basic BJT current mirror, Widlar current source, Wilson current mirror, basic MOS current mirror, cascoded current mirror, output resistance, current mirror accuracy and limitations, and applications of current mirrors in analog integrated circuits.

Prescribed Textbooks:

Sl. No.	Book Title	Authors	Edition	Publisher	Year
1	Electronic Principles	Albert Malvino, David j Bates, Patrick E. Hoppe	9th	McGraw-Hill Education	2021
2.	Microelectronic Circuits, Theory and Applications	Adel S. Sedra Kenneth C. Smith	7th	Oxford university press	2009
3.	Design of Analog CMOS Integrated Circuits	Behzad Razavi	2nd	McGraw-Hill Education	2017

Reference Books:

Sl. No	Book Title	Authors	Edition	Publisher	Year
1.	Fundamentals of Microelectronics	Behzad Razavi	2nd	Wiley India Pvt. Ltd	2014
2.	Electronic Devices and Circuits Theory	Robert L. Boylestad and Louis Nashelsky	10th	Pearson,	2012
3.	Op Amps and Linear Integrated Circuits	Ramakant A Gayakwad	4th	Pearson Education	2015

Weblinks and Video Lectures(e-Resources):

- https://nptel.ac.in/courses/108102112
- https://onlinecourses.nptel.ac.in/noc25_ee157/preview
- https://nptel.ac.in/courses/108106188

Teaching-Learning–Evaluation Scheme:

Sl. No	Teaching and Learning Method	No. of Hours/ Week	No. of Weeks	Hours/ Semester
1.	Classroom Teaching & Learning	3	14	42
2.	Evaluation of Learning Process	-	-	10
3.	Integrated Lab (Fixed Experiments)	2	14	28
4.	Integrated Lab (Open-ended Experiments)	-	-	40
Total Learning Hours/Semester				**120**

Proposed Assessment Plan (for 50 marks of CIE):

Tool	Remarks	Marks
CIE	Two CIEs conducted for 50 marks each and reduced to 15 marks	30
Activity Details	Integrated lab experiments	20

Integrated lab experiments:

Sl. No.	PART-A: Fixed Experiments
1	Design and analyze a Base-Biased Common-Emitter (CE) Amplifier and determine voltage gain, input impedance, and output impedance.
2	Design and analyze an Emitter-Biased Common-Emitter Amplifier and study the effect of emitter resistance on amplifier performance.
3	Simulate and analyze Common-Collector (Emitter Follower) and Common-Base Amplifiers and compare their characteristics.
4	Design and analyze a Darlington Amplifier and evaluate its current gain and input impedance.
5	Design and simulate a Common-Source MOSFET Amplifier and determine voltage gain and frequency response.
6	Design and analyze a Source Follower (Common-Drain) MOSFET Amplifier and study its voltage gain and output impedance.
7	Design and simulate a Negative Feedback Amplifier and compare the gain, bandwidth, and stability with an open-loop amplifier.
8	Design and simulate an RC Phase-Shift or Wien Bridge Oscillator and verify the conditions for sustained oscillations.
9	Design and analyze Class A and Class B Power Amplifiers and compare efficiency and output characteristics.
10	Design and simulate a BJT and MOSFET Current Mirror and study current regulation characteristics.
Sl. No.	**PART-B: Open-ended Experiments**
1	Design a multistage BJT voltage amplifier to achieve a specified voltage gain and bandwidth.
2	Design a MOSFET amplifier with a specified voltage gain using an appropriate biasing technique and compare simulation and theoretical results.
3	Design and optimize a negative feedback amplifier to achieve a specified gain and bandwidth.
4	Design an Oscillator Using an Op-Amp- Design a Wien bridge or RC oscillator to generate a specified output frequency.
5	Design a constant current source using BJT or MOSFET for a specified load current.
6	Design and analyze a Wilson or Widlar Current Mirror and compare its performance with a basic current mirror.

Course Articulation Matrix:

Course Outcomes	Program Outcomes												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO 2**
CO1	3	2	-	-	-	-	-	-	-	-	-	2	-
CO2	2	3	2	1	3	-	-	1	1	-	-	2	-
CO3	2	2	3	1	2	-	-	1	-	-	-	3	-
CO4	2	3	2	2	3	-	-	1	1	-	1	2	-

Course Title	DIGITAL ELECTRONICS		
Course Code	25VL303	(L-T-P) C	(3-0-0)3
Exam	3 hours	Hours/Week	3 hours
SEE	50 marks	Total Hours	42L+38ABL+10EV

Course Objective: To provide a strong foundation in digital electronics through the analysis and design of combinational and sequential logic circuits. The course enables students to apply Boolean algebra, programmable logic devices, counters, and finite state machines for the development of digital systems relevant to VLSI and embedded applications.

Course Outcomes: with mapping shown against the Program Outcomes (POs)}

Upon completion of the course, students shall be able to:

CO's	Course Outcomes	Mapping to POs	Mapping to PSOs
1.	Apply Boolean algebra and logic minimization techniques to simplify and implement combinational logic circuits.	1, 2, 3	1
2.	Design combinational digital circuits using adders, subtractors, multiplexers, decoders, encoders, and programmable logic devices.	1, 2, 3, 5, 8, 9	1
3.	Analyze sequential logic circuits using latches, flip-flops, registers, and shift registers.	1, 2, 3,5	1
4.	Design synchronous counters and finite state machines (Mealy and Moore) for digital system applications	1, 2, 3, 4 5, 8, 9	1, 2

Course Contents:

Module1	10 Hours

Simplification of Boolean Functions: Minterm canonical form and m-notation, Maxterm canonical form and M-notation, Map method-2, 3 and 4 variables, Product and sums simplification, don't care conditions, NAND and NOR implementation, 3 and 4 variable Tabulation method**.**

Module2	10 Hours

Combinational Circuits Design and Analysis: Parallel adder, Parallel subtractor, carry look ahead adder, BCD adder, magnitude comparator, encoder, priority encoder, decoder, multiplexer, de-multiplexer, Arithmetic circuits and code converters using Multiplexers and Decoders.

Module3	11 Hours

Programmable Logic Devices and Flip-Flops: Introduction to Programmable Logic Devices, Programmable Logic Arrays (PLA), Programmable Array Logic (PAL), Basic Bistable element, Latches and Flip Flops- SR, JK, D, T, Master-slave JK flip-flop, Characteristic equations of Flip-Flops, Triggering of Flip Flops, Flip Flop Excitation Tables.

Sequential Circuits-I: Registers (SISO, PISO), Universal Shift Register, Counters - Synchronous and Asynchronous counters, Design of Asynchronous Binary counters.

MODULE-4	11 Hours

Sequential Circuits-II: Design of a Synchronous mod-N counter using clocked SR, JK, and T flip-flops, Analysis of Synchronous Binary counters, Mealy and Moore models, Analysis of Sequential Circuits, Analysis of Clocked Synchronous Sequential Circuits, Sequence Detector.

Prescribed Textbooks:

Sl. No.	Book Title	Authors	Edition	Publisher	Year
1.	Digital Design	M Morris Mano	5th	Pearson Edition	2013
2.	Digital Principles and design	Donald D Givone	1st	McGraw-Hill	2017

Reference Books:

Sl. No	Book Title	Authors	Edition	Publisher	Year
1.	Digital Logic Applications and Design	John M Yarbrough	1st	Cengage learning India	2006
2.	Logic Design	R D Sudhakar Samuel	1st	Pearson Edition	2007

Web links and Video Lectures (e-Resources):

1. https://www.youtube.com/watch?v=CICw_06v68Y&list=PLbRMhDVUMngePP5JcezxImF-FzOC9wstz&index=2.
2. https://www.youtube.com/watch?v=LuvIPkYJxsU&list=PLbRMhDVUMngePP5JcezxImF-FzOC9wstz&index=3.
3. https://onlinecourses.nptel.ac.in/noc20_ee32/preview.
4. National Instruments: https://education.ni.com/teach/resources/1104/digital-electronics.

Teaching-Learning–Evaluation Scheme:

Sl. No	Teaching and Learning Method	No. of Hours/ Week	No. of Weeks	Hours/ Semester
1.	Classroom Teaching &Learning	3	14	42
2.	Activity Based Learning (ABL1&ABL2)	-	-	38
3.	Evaluation of Learning Process	-	-	10
Total Learning Hours/Semester				**90**

Proposed Assessment Plan (for 50 marks of CIE):

Tool	Remarks	Marks
CIE	Two tests conducted for 50 marks each and reduced to 15 marks	30
Activity Details	Details of activities to be conducted **Activity 1:** Logic Design and Simulation of combinational circuits- 10 marks 1) Design and simulate combinational circuits such as adders, multiplexers, decoders, flip-flops, registers, and counters using Logisim Evolution or Multisim	20

	2) Verify the functionality using truth tables, Karnaugh maps, timing diagrams, and simulation waveforms. **Activity 2:** Design and Simulation of sequential circuits- 10 marks Design and simulate sequential logic circuits and verify the functionality.	
Total		**50**

Activity Based Learning (38Hours)

ABL 1- Logic Design and Simulation of combinational circuits		**Hours**
Design and Simulation of combinational circuits	Simulation of digital circuits	6
	Preparation and planning for simulation activities	6
	Execution and verification of simulation results	4
	Documentation of simulation outcomes	4
Total		**20**
ABL 2- Design and Simulation of sequential circuits		
Design and Simulation of sequential circuits	Simulation of digital circuits	6
	Preparation and planning for simulation activities	6
	Execution and verification of simulation results	2
	Documentation of simulation outcomes	4
Total		**18**

Evaluation of Learning Process (10Hours)

Type of Evaluation	**Hours**
CIE (1 and 2)	3
Demonstration of activity and report submission	4
Semester End Exam	3
Total	**10**

Course Articulation Matrix

Course Outcomes	**Program Outcomes**												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**
CO1	3	2	2	-	-	-	-	-	-	-	-	2	-
CO2	3	3	3	-	3	-	-	2	2	-	-	3	-
CO3	3	3	2	-	3	-	-	-	-	-	-	3	-
CO4	2	2	3	2	3	-	-	2	2	-	-	2	3

Course Title	DIGITAL SYSTEM DESIGN USING VERILOG		
Course Code	25VL304	(L-T-P) C	(3-0-0)3
Exam	3 hours	Hours/Week	3 hours
SEE	50 marks	Total Hours	42L+38ABL+10EV

Course Objective: To introduce students to the fundamentals of Verilog HDL and digital design methodologies for modeling combinational and sequential circuits. The course enables students to develop, simulate, and verify digital designs using structural, dataflow, and behavioral modeling techniques.

Course Outcomes: with mapping shown against the Program Outcomes (POs)
Upon completion of the course, students shall be able to:

CO's	Course Outcomes	Mapping to POs	Mapping to PSOs
1.	Explain the fundamentals of Verilog HDL, hierarchical design methodology, modules, ports, data types, and simulation concepts.	1, 2, 5	1
2.	Develop Verilog models for combinational logic circuits using gate-level and dataflow modeling techniques.	1, 2, 3, 4, 5	1
3.	Design and implement digital systems using behavioral modeling, tasks, functions, and procedural constructs in Verilog HDL.	1, 2, 3, 4, 5, 8, 11	1
4.	Design, simulate, and verify finite state machines (FSMs) and digital circuits using Verilog HDL, applying timing specifications and simulation techniques	1, 2, 3, 4, 5, 8, 9, 11	1, 2

Course Contents:

Module1	11 Hours

Overview of Digital Design with Verilog HDL: Evolution of CAD, emergence of HDLs, typical HDL-flow, why Verilog HDL? Trends in HDLs). Hierarchical Modeling Concepts: Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block. Lexical conventions, data types, system tasks, compiler directives.

Module2	10 Hours

Modules and Ports: Module definition, port declaration, connecting ports, hierarchical name referencing. **Gate-Level Modeling:** Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays.

Module3	10 Hours

Modeling: Dataflow Modeling- Continuous assignments, delay specification, expressions, operators, operands, operator types. **Behavioral Modeling:** Structured procedures, initial and always, blocking and non-blocking statements, delay control, Multiway branching, loops, sequential and parallel blocks.
Tasks and functions.

MODULE-4	11 Hours

FSM and Modeling Techniques: Implementation of FSM using Verilog, examples: Sequence detector, Traffic light controller. Procedural continuous assignments, overriding parameters, conditional compilation and execution, useful system tasks. Timing and Delays-Distributed, lumped and pin-to-pin delays, specify blocks, parallel and full connection, timing checks, delay back-annotation.

Prescribed Textbooks:

Sl. No.	Book Title	Authors	Edition	Publisher	Year
1.	Verilog HDL: A Guide to Digital Design and Synthesis	Samir Palnitkar	2nd	Pearson Education	2003

Reference Books:

Sl. No	Book Title	Authors	Edition	Publisher	Year
1.	The Verilog Hardware Description Language	Donald E. Thomas, Philip R. Moorby	5th	Springer	-
2.	Design through Verilog HDL	T.R. Padmanabhan, B. Bala Tripura Sundari	1st	Wiley Publication	2008

E-Books and Online course material:

1. https://rashmistudents.yolasite.com/resources/Verilog%20HDL%20-%20Samir%20Palnitkar.pdf
2. https://www.slideshare.net/slideshow/solutions-of-sedra-and-smith/54332123

Online course and video lecture:

1. https://nptel.ac.in/courses/117106086
2. https://www.digimat.in/nptel/courses/video/108105113/L27.html
3. http://www.ece.ubc.ca/~saifz/eece256.html

Teaching-Learning–Evaluation Scheme:

Sl. No	Teaching and Learning Method	No. of Hours/ Week	No. of Weeks	Hours/ Semester
1.	Classroom Teaching &Learning	3	14	42
2.	Activity Based Learning (ABL1&ABL2)	-	-	38
3.	Evaluation of Learning Process	-	-	10
Total Learning Hours/Semester				**90**

Proposed Assessment Plan (for 50 marks of CIE):

Tool	Remarks	Marks
CIE	Two tests conducted for 50 marks each and reduced to 15 marks	30
Activity Details	Details of activities to be conducted: **Activity1**- Simulation-based activity involves using software tools to create and test digital circuits in a virtual environment (10 Marks). **Activity2**- Poster Presentation (10 Marks).	20
Total		**50**

Activity Based Learning (38Hours)

ABL1-Simulation-Based Activity:		**Hours**
A simulation-based activity involves using software tools to design and test digital circuits in a virtual environment	Simulation of digital systems using Verilog HDL concepts	6
	Preparation and planning for simulation activities	6
	Execution and verification of simulation results	4
	Documentation of simulation outcomes	4
Total		**20**
ABL2- Poster Presentation:		
Presents HDL design, Verilog implementation, and verification results through a clear and informative poster.	Presents HDL design concepts, Verilog implementation, and verification results.	4
	Arrange information using a clear structure, diagrams, and visual elements.	7
	Explain the poster effectively and respond to technical queries.	7
Total		**18**

Evaluation of Learning Process (10Hours)

Type of Evaluation	**Hours**
CIE (1 and 2)	3
Demonstration of activity and report submission	4
Semester End Exam	3
Total	**10**

Course Articulation Matrix

Course Outcomes	**Program Outcomes**												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**
CO1	3	2	-	-	2	-	-	-	-	-	-	2	-
CO2	3	3	2	1	3	-	-	-	-	-	-	3	-
CO3	3	2	3	2	3	-	-	1	-	-	1	3	-
CO4	3	3	3	2	3	-	-	1	1	-	1	3	3

Course Title	Physics of semiconductor devices		
Course Code	25VL305	(L-T-P) C	(3-0-0)3
Exam	3 hours	Hours/Week	3 hours
SEE	50 marks	Total Hours	42L + 48ABL = 90

Course Objective: To provide a fundamental understanding of semiconductor materials, PN junctions, BJTs, JFETs, and MOSFETs, along with their operating principles and characteristics. To introduce semiconductor device fabrication processes and advanced MOS devices such as FinFETs used in modern VLSI technology.

Course Outcomes: with mapping shown against the Program Outcomes (POs)
Upon completion of the course, students shall be able to:

CO's	Course Outcomes	Mapping to POs	Mapping to PSOs
1.	Describe the fundamental concepts of semiconductor materials, energy bands, charge carriers, conductivity, mobility, and Hall Effect.	1, 2	1
2.	Analyze the operation and characteristics of PN junctions, rectifiers, optoelectronic devices, and Bipolar Junction Transistors.	1, 2, 3, 5	1
3.	Analyze the structure, operation, and current-voltage characteristics of JFETs and MOSFETs.	1, 2, 3, 5	1
4.	Describe semiconductor fabrication processes and assess the structure, operation, advantages, and applications of FinFET devices.	1, 2	1

Course Contents:

Module1	11 Hours

Semiconductors and PN Junctions: Bonding forces in solids, Energy bands, Metals, Semiconductors and Insulators, Direct and Indirect semiconductors, Electrons and Holes, Intrinsic and Extrinsic materials, Conductivity and Mobility, Drift and Resistance, Effects of temperature and doping on mobility, Hall Effect. **PN Junctions:** Forward and Reverse biased junctions, Qualitative description of Current flow at a junction, Reverse bias, Reverse bias breakdown, Zener breakdown, Avalanche breakdown, Rectifiers.

Module2	11 Hours

Optoelectronic Devices and Bipolar Junction Transistor: Optoelectronic Devices: Photodiodes: Current and Voltage in an Illuminated Junction, Solar Cells, Photodetectors, Light Emitting Diode, Light Emitting materials. **Bipolar Junction Transistor:** Fundamentals of BJT operation, Amplification with BJTs, BJT Fabrication, the coupled Diode model (Ebers-Moll Model), Switching operation of a transistor, Cutoff, Saturation, Switching cycle, Specifications, Drift in the base region, Base narrowing, Avalanche breakdown.

Module3	10 Hours

Field Effect Transistors: Basic pn JFET Operation, Equivalent Circuit and Frequency Limitations, **MOSFET:** Two-terminal MOS structure, Energy band diagram, Ideal Capacitance-Voltage Characteristics and Frequency Effects, Basic MOSFET Operation, MOSFET structure, Current-Voltage Characteristics.

MODULE-4	10 Hours

Fabrication process: Thermal Oxidation, Diffusion, Rapid Thermal Processing, Ion implantation, Chemical Vapour Deposition, Photolithography, Etching, Metallization.
Advanced MOS Devices: FinFET Structure and Operation, Advantages of FinFET over Planar MOSFET, Applications of FinFET in Modern VLSI Technology.

Prescribed Textbooks:

Sl. No.	Book Title	Authors	Edition	Publisher	Year
1.	Solid State Electronic Devices	Ben G. Streetman and Sanjay Banerjee	7th	Pearson Education	2015
2.	Semiconductor Physics and Devices: Basic Principles	Donald A. Neamen	4th	McGraw-Hill Education	2012

Reference Books:

Sl. No	Book Title	Authors	Edition	Publisher	Year
1.	Fundamentals of Modern VLSI Devices.	Yuan Taur and Tak H. Ning,	2nd	Cambridge University Press	2009
2.	Physics of Semiconductor Devices	Simon M. Sze and Kwok K. Ng	3rd	John Wiley & Sons	2007
3.	Modern Semiconductor Devices for Integrated Circuits	Chenming Hu	1st	Pearson Education	2010

Weblinks and Video Lectures(e-Resources):

1. https://nptel.ac.in/courses/108103009
2. https://nanohub.org
3. https://ocw.mit.edu/courses/6-012-microelectronic-devices-and-circuits-fall-2009/
4. https://www.allaboutcircuits.com/textbook/semiconductors/
5. https://www.coursera.org/learn/semiconductor-devices

Teaching-Learning–Evaluation Scheme:

Sl. No	Teaching and Learning Method	No. of Hours/ Week	No. of Weeks	Hours/ Semester
1.	Classroom Teaching &Learning	3	14	42
2.	Activity Based Learning (ABL1&ABL2)	-	-	38
3.	Evaluation of Learning Process	-	-	10
Total Learning Hours/Semester				**90**

Proposed Assessment Plan (for 50 marks of CIE):

Tool	Remarks	Marks
CIE	Two tests conducted for 50 marks each and reduced to 15 marks	30
Activity Details	**Activity 1:** Simulation of PN Junction Diode Characteristics **Activity 2:** Seminar/Presentation on Modern Transistor Technologies	20
Total		**50**

Activity Based Learning (38Hours)

ABL1-Simulation-Based Activity:		**Hours**
Simulation of PN Junction Diode Characteristics	Simulation of PN Junction Diode Characteristics	6
	Preparation and planning for simulation activities	6
	Execution and verification of simulation results	4
	Documentation of simulation outcomes	4
Total		**20**
ABL2- Presentation:		
Seminar/Presentation on Modern Transistor Technologies	Collection of information and slide preparation	4
	Arrange information using a clear structure, diagrams, and visual elements.	7
	Explain the concepts effectively and respond to technical queries.	7
Total		**18**

Evaluation of Learning Process (10Hours)

Type of Evaluation	**Hours**
CIE (1 and 2)	3
Demonstration of activity and report submission	4
Semester End Exam	3
Total	**10**

Course Articulation Matrix

Course Outcomes	**Program Outcomes**												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**
CO1	3	2	-	-	-	-	-	-	-	-	-	2	-
CO2	3	3	2	-	2	-	-	-	-	-	-	3	-
CO3	3	3	2	-	2	-	-	-	-	-	-	3	-
CO4	3	3	-	-	-	-	-	-	-	-	-	3	-

Course Title	Digital system design using Verilog Lab		
Course Code	25VL306	(L-T-P) C	(0-0-2)1
Exam	3	Hours/Week	2
SEE	50 marks	Total Hours	28P+2E=30

Course objectives: To provide students with practical knowledge of Verilog HDL for modeling, simulating, and verifying combinational and sequential digital circuits. The course enables students to design, implement, validate, and optimize digital systems using industry-standard HDL practices while developing problem-solving skills through open-ended hardware design experiments.

Course Outcomes (COs): Upon completion of the course, students shall be able to:

COs	Statement	POs	PSOs
1.	Design, model, simulate, and verify combinational digital circuits using Verilog HDL and appropriate test benches.	1, 2, 3, 4, 5, 8, 9, 11	1, 2
2.	Design and analyze sequential digital circuits, including flip-flops, counters, and finite state machines, using Verilog HDL.	1, 2, 3, 4, 5, 8, 9, 11	1, 2
3.	Develop, implement, and validate complex digital systems such as ALUs, arithmetic circuits, and application-oriented hardware solutions using Verilog HDL to solve open-ended design problems.	1, 2, 3, 4, 5, 8, 9, 11	1, 2

ABL: Lab based learning (28Hrs.)

Sl. No.	PART-A: Fixed Experiments
1	Design and verify logic gates using Verilog HDL.
2	Design a 2-to-4 Decoder and an 8-to-3 Encoder (with and without priority).
3	Design an 8-to-1 Multiplexer using behavioral modeling (case and if) and implement a Binary-to-Gray code converter.
4	Design and verify Half Adder, Full Adder, and 1-bit Adder-Subtractor.
5	Design a 4-bit Ripple Carry Adder and Carry Look-Ahead Adder.
6	Design and verify SR, JK, D, and T Flip-Flops.
7	Design Synchronous and Asynchronous 4-bit Binary/BCD Counters.
8	Design a Clock Divider to generate divide-by-2, divide-by-4, divide-by-8, and divide-by-16 clocks.
9	Design and verify a 4-bit Multiplier and 4-bit Divider.

10	Design a Finite State Machine (Mealy and Moore) for sequence detection.
Sl. No.	**PART-B: Open-ended Experiments**
1	Design an Arithmetic Logic Unit (ALU) supporting at least eight operations using behavioral or structural modeling.
2	Design a Digital Traffic Light Controller with pedestrian crossing support.
3	Design an Elevator Controller for a four-floor building using FSM.
4	Design a Stopwatch/Timer with Start, Stop, Pause, and Reset controls.
5	Design a UART Transmitter or Receiver for serial communication.
6	Design a Simple Vending Machine Controller using FSM with change return logic.

Proposed Assessment Plan for 50 marks:

Tool	Remarks	Marks
Assessment method	Continuous Evaluation Record Writing Lab CIE	10 20 20
Total		**50**

Teaching-Learning–Evaluation Scheme:

Sl. No	Teaching and Learning Method	No. of Hours/Week	No. of Weeks	Hours/ Semester
1	Lab Conduction	2	14	28
2	Evaluation	-	-	02
Total Learning Hours/Semester				30

Reference Books:

1. **Nazeih M. Botors**–"HDL Programming (VHDL and Verilog)", Dream tech publication New Delhi.
2. **J Bhaskar**, "VHDL Primer", Pearson/PHI, New Delhi 2003.

Online Courses and Video Lectures:

1. https://onlinecourses.nptel.ac.in/noc24_cs61/preview?utm_source=chatgpt.com
2. https://onlinecourses.nptel.ac.in/noc25_ee180/preview?utm_source=chatgpt.com

Course Articulation Matrix:

Course Outcomes	Program Outcomes												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**
CO1	3	2	3	1	3	-	-	2	1	-	1	2	2
CO2	3	2	2	2	3	-	-	2	2	-	2	3	2
CO3	2	2	3	2	3	-	-	2	2	-	3	3	3

Course Title	Linux Programming Laboratory		
Course Code	25VL307A	**(L-T-P) C**	(0-0-2) 1
Exam	3 Hours	**Hours/Week**	2 Hrs.
SEE	50 Marks	**Total Hours**	28P+2E=30

Course Objective: To provide students with practical knowledge of the Linux operating system, command-line environment, and scripting using Shell, Tcl, and Perl. The course enables students to develop automation scripts, solve application-oriented problems, and support Linux-based VLSI/EDA workflows through open-ended programming and system administration tasks.

Course Outcomes: At the end of the course, students shall be able to:

#	Course Outcomes	Mapping to PO's	Mapping to PSO's
1	Demonstrate proficiency in using Linux commands, file systems, process management, and system utilities to perform programming and system administration tasks.	1, 2, 5, 8, 9	1
2	Develop and debug Shell, Tcl, and Perl scripts to automate tasks and solve engineering problems in the Linux environment.	1, 2, 3, 4, 5, 8, 9, 11	1
3	Design, implement, and evaluate Linux-based scripting solutions for application-oriented and open-ended problems, including automation and VLSI/EDA support tasks.	1, 2, 3, 4, 5, 8, 9, 11	1

ABL: Lab based learning (28 Hrs.)

Conduct the following experiments using the required software tool:

Sl. No.	PART-A: Fixed Experiments
1	Introduction to Linux operating system, terminal, directory structure, and file system.
2	Practice Linux file and directory management commands (pwd, ls, cd, mkdir, cp, mv, rm, cat).
3	Perform file permission management and use Linux filters (chmod, grep, sort, wc, head, tail).
4	Develop Shell scripts using variables, input/output, arithmetic operations, and command-line arguments.
5	Develop Shell scripts using conditional statements (if, case).
6	Develop Shell scripts using loops (for, while) and user-defined functions.
7	Develop Tcl programs using variables, operators, and input/output operations.
8	Develop Tcl programs using control statements, procedures, lists, arrays, and file handling.

9	Develop Perl programs using scalars, arrays, operators, control structures, and subroutines.
10	Develop Perl programs for file handling and text processing using regular expressions.
Sl. No.	**PART-B: Open-ended Experiments**
1	Develop a Shell script to automate file backup and restoration.
2	Develop a Shell utility to monitor CPU, memory, and disk utilization.
3	Develop a Tcl program for automated configuration file generation.
4	Develop a Perl script to extract and summarize information from large text files.
5	Design a Linux automation tool to organize files based on extension, size, or date.
6	Develop a script to automate execution of multiple Linux commands for software installation or project setup.

Proposed Assessment Plan (for 50 marks of CIE):

Tool	Remarks	Marks
CIE	Continuous evaluation	10
	Record writing	20
	Lab CIE	20
	Total	**50**

Teaching - Learning – Evaluation Scheme:

Sl. No	Teaching and Learning Method	No. of Hours/Week	No. of Weeks	Hours/Semester
1	Lab conduction	2	14	28
2	Evaluation	-	-	02
Total Learning Hours/Semester				30

Prescribed Textbooks:

Sl. No	Book Title	Authors	Edition	Publisher	Year
1	The Linux Command Line: A Complete Introduction	William E. Shotts Jr.	2nd	No Starch Press	2019
2	UNIX and Shell Programming	B. A. Forouzan & Richard F. Gilberg	1st	Cengage Learning	2003
3	Learning Perl	Randal L. Schwartz, Tom Phoenix & brian d foy	8th	O'Reilly Media	2021

eBooks and online course materials:

1. https://linuxcommand.org/tlcl.php
2. https://training.linuxfoundation.org/resources/

Online Courses and Video Lectures:

1. https://nptel.ac.in/courses/106106144
2. https://training.linuxfoundation.org/training/introduction-to-linux/
3. https://www.youtube.com/playlist?list=PLS1QulWo1RIZcKJ9Qj7xT0M6Y4vC0Z8xK&

Course articulation Matrix

Course Outcomes	Program Outcomes												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**
CO1	2	2	-	-	3	-	-	2	1	-	-	2	-
CO2	2	3	2	1	3	-	-	2	1	-	2	2	-
CO3	2	3	2	2	3	-	-	2	2	-	2	3	-

Course Title	PROGRAMMABLE LOGIC CONTROLLER		
Course Code	25VL407B	**(L-T-P) C**	(0-0-2)1
Exam	3	**Hours/Week**	2
SEE	50 marks	**Total Hours**	28P+2E=30

Course Objective: To provide students with practical knowledge of Programmable Logic Controllers (PLCs) for industrial automation through ladder logic programming and implementation. The course enables students to develop, test, troubleshoot, and optimize PLC-based control systems using timers, counters, arithmetic, comparison, and PID instructions to solve application-oriented open-ended industrial automation problems.

Course Outcomes (COs) {with mapping shown against the Program Outcomes (POs)}

Upon completion of the course, students shall be able to:

COs	Statement	POs	PSOs
1.	Demonstrate proficiency in PLC hardware, software environment, and ladder logic programming using fundamental PLC instructions.	1, 2, 5, 8	1
2.	Develop, implement, and test PLC ladder logic programs using timers, counters, arithmetic, comparison, and logical instructions for industrial automation applications.	1, 2, 3, 4, 5, 8, 9	1
3.	Design, implement, and evaluate PLC-based automation solutions for application-oriented and open-ended industrial control problems using appropriate programming, testing, and troubleshooting techniques.	1, 2, 3, 4, 5, 8, 9	1

ABL: Lab based learning (28Hrs.)

Sl. No.	PART-A: Fixed Experiments
1	Study the hardware architecture, input/output modules, and programming software of a PLC system.
2	Develop and execute simple PLC ladder logic programs using basic logic instructions.
3	Develop a PLC ladder logic program for a Direct-On-Line (DOL) motor starter.
4	Develop PLC applications using On-Delay (TON) and Off-Delay (TOF) timers.
5	Develop PLC applications using Up (CTU) and Down (CTD) counters.
6	Implement arithmetic and computational instructions in PLC ladder logic.

7	Implement comparison and logical instructions in PLC ladder logic.
8	Develop a PLC program for sequence control of an industrial process.
9	Develop a PLC program for conveyor belt control with object counting.
10	Develop and verify a PLC program for a Traffic Light Control System.
Sl. No.	**PART-B: Open-ended Experiments**
1	Design a PLC-based automatic water tank level control system.
2	Develop a PLC program for an automatic bottle filling system.
3	Design a PLC-based car parking management system with vehicle counting.
4	Develop a PLC program for an elevator control system.
5	Design a PLC-based automatic street lighting system using sensor inputs.
6	Develop a PLC program for a three-phase motor protection and monitoring system.

Proposed Assessment Plan for 50 marks:

Tool	Remarks	Marks
Assessment method	Continuous Evaluation Record writing Lab CIE	10 20 20
Total		**50**

Teaching-Learning–Evaluation Scheme:

Sl. No	Teaching and Learning Method	No. of Hours/Week	No. of Weeks	Hours/ Semester
1	Lab Conduction	2	14	28
2	Evaluation	-	-	02
Total Learning Hours/Semester				30

Textbook:

Sl. No	Book Title	Authors	Edition	Publisher	Year
1	Programmable Logic Controllers	Frank D. Petruzella	5th	McGraw-Hill Education	2017

Reference Books:

Sl. No	Book Title	Authors	Edition	Publisher	Year
1	Programmable Logic Controllers: Principles and Applications	John W. Webb and Ronald A. Reis	5th	PHI Learning	2017
2	Introduction to Programmable Logic Controllers	Gary Dunning	3rd	Cengage Learning	2005

eBooks and online course materials:

1. https://nptel.ac.in/courses/108/105/108105129/ (NPTEL – Programmable Logic Controllers and their Industrial Applications, IIT Kanpur)

Online Courses and Video Lectures:

1. https://www.youtube.com/watch?v=BHv6S2Kk1T8
2. https://www.youtube.com/watch?v=BHv6S2Kk1T8&utm_source

Course Articulation Matrix:

Course Outcomes	Program Outcomes												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**
CO1	2	3	-	-	3	-	-	2	-	-	1	2	2
CO2	2	3	3	2	3	-	-	2	1	-	1	2	3
CO3	2	2	3	2	3	-	-	2	2	-	1	2	3

Course Title	Simulation of Circuits and Devices		
Course Code	25VL307C	(L-T-P) C	(0-0-2)1
Exam	3	Hours/Week	2
SEE	50 marks	Total Hours	28P+2E=30

Course Objective: To provide students with practical knowledge of schematic capture and electronic circuit simulation using industry-standard EDA tools. The course enables students to design, simulate, analyze, validate, and optimize semiconductor devices and electronic circuits through DC, AC, and transient analyses while solving application-oriented open-ended circuit design problems.

Course Outcomes (COs) with mapping shown against the Program Outcomes (POs)

Upon completion of the course, students shall be able to:

COs	Statement	POs	PSOs
1.	Design and simulate basic analog and digital electronic circuits using schematic capture and electronic circuit simulation tools.	1, 2, 3, 4, 5, 8, 9	1
2.	Analyze the characteristics of semiconductor devices and evaluate the DC, AC, and transient responses of electronic circuits through simulation.	1, 2, 3, 4, 5, 8, 9, 11	1
3.	Design, validate, and optimize application-oriented electronic circuits using simulation tools to solve open-ended engineering problems through performance analysis and verification.	1, 2, 3, 4, 5, 8, 9, 11	1

ABL: Lab based learning (28Hrs.)

Sl. No.	PART-A: Fixed Experiments
1	Familiarization with schematic capture and electronic circuit simulation software.
2	Draw and simulate a resistor network to verify Ohm's Law and Kirchhoff's Laws.
3	Draw and simulate a PN junction diode circuit to obtain V-I characteristics.
4	Draw and simulate a Zener diode voltage regulator and study its characteristics.
5	Draw and simulate a BJT circuit to obtain input and output characteristics.
6	Draw and simulate a MOSFET circuit to obtain transfer and output characteristics.
7	Draw and simulate a Common-Emitter BJT amplifier and analyze its gain and frequency response.
8	Draw and simulate a Common-Source MOSFET amplifier and analyze its performance.
9	Draw and simulate RC low-pass and high-pass filters and analyze frequency and transient responses.

10	Draw and simulate half-wave and full-wave bridge rectifier circuits and analyze their output waveforms.
Sl. No.	**PART-B: Open-ended Experiments**
1	Design and simulate a regulated DC power supply using rectifier, filter, and voltage regulator circuits.
2	Design and simulate a transistor-based electronic switching circuit for industrial applications.
3	Design and simulate a multi-stage amplifier to achieve a specified voltage gain.
4	Design and simulate an active low-pass or high-pass filter for a given cutoff frequency.
5	Design and simulate a waveform generator using analog circuit components.
6	Design and simulate a transistor-based LED driver or relay driver circuit.

Proposed Assessment Plan for 50 marks:

Tool	Remarks	Marks
Assessment method	Continuous Evaluation Record writing Lab CIE	10 20 20
Total		**50**

Teaching-Learning–Evaluation Scheme:

Sl. No	Teaching and Learning Method	No. of Hours/Week	No. of Weeks	Hours/ Semester
1	Lab Conduction	2	14	28
2	Evaluation	-	-	02
Total Learning Hours/Semester				30

Textbook:

Sl.No	Book Title	Authors	Edition	Publisher	Year
1.	Microelectronic Circuits	A. S. Sedra and K. C. Smith	7th	Oxford University Press	2015
2.	Electronic Devices and Circuit Theory	R. L. Boylestad and L. Nashelsky	11th	Pearson Education	2015

Reference books:

1. LTspice XVII User Guide and Help Manual. Wilmington, MA, USA: https://www.analog.com/en/resources/design-tools-and-calculators/ltspice-simulator.html
2. J. W. Eaton, D. Bateman, S. Hauberg, and the ngspice Development Team, *Ngspice User's Manual*, Version 46. [Online]. Available: https://ngspice.sourceforge.io/docs.html

Web links and Video Lectures (e-Resources):

1. MIT Open Course Ware – Circuit simulation lectures https://ocw.mit.edu/courses/6-002-circuits-and-electronics-spring-2007/resources/lecture-videos/
2. All About Circuits – SPICE tutorials https://www.allaboutcircuits.com/textbook/product/circuit-simulation/

Course Articulation Matrix

Course Outcomes	Program Outcomes												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**
CO1	3	2	2	1	3	-	-	2	1	-	-	2	-
CO2	3	3	2	2	3	-	-	2	1	-	2	3	-
CO3	2	2	2	3	3	-	-	2	2	-	2	3	-

Course Title	Numerical Computing Laboratory using GNU Octave / Scilab		
Course Code	25VL307D	**(L-T-P) C**	(0-0-2)1
Exam	3	**Hours/Week**	2
SEE	50 marks	**Total Hours**	28P+2E=30

Course Objective: To provide students with practical knowledge of GNU Octave/Scilab for numerical computing, scientific programming, mathematical modeling, and data visualization. The course enables students to develop algorithms, analyze engineering data, and solve application-oriented open-ended numerical computing problems using scientific programming techniques.

Course Outcomes (COs) with mapping shown against the Program Outcomes (POs)

Upon completion of the course, students shall be able to:

COs	Statement	POs	PSOs
1.	Develop and execute GNU Octave/Scilab programs to perform numerical computations and solve engineering problems using appropriate programming constructs.	1, 2, 4, 5, 8, 9	1
2.	Apply GNU Octave/Scilab for matrix operations, mathematical modeling, signal generation, and visualization of engineering data.	1, 2, 3, 4, 5, 8, 11	1
3.	Design, implement, and evaluate application-oriented numerical computing solutions using GNU Octave/Scilab to solve open-ended engineering problems through algorithm development and scientific analysis.	1, 2, 3, 4, 5, 8, 9, 11	1

ABL: Lab based learning (28Hrs)

Sl. No.	PART-A: Fixed Experiments
1	Introduction to GNU Octave/Scilab environment, commands, variables, and workspace.
2	Matrix and vector operations using built-in functions.
3	Development of scripts for mathematical computations and user-defined functions.
4	Programs using conditional statements (if, switch) for engineering applications.
5	Programs using iterative statements (for, while) for numerical computations.
6	Plotting of mathematical functions using 2D plotting commands.
7	Generation and visualization of sine, cosine, and other periodic signals.
8	Multiple plots, subplot, legends, annotations, and graphical formatting.
9	Signal operations such as addition, scaling, shifting, and multiplication.

10	Solving systems of linear equations and visualization of exponential, logarithmic, and frequency response characteristics.
Sl. No.	**PART-B: Open-ended Experiments**
1	Develop a program to solve roots of nonlinear equations using any numerical method.
2	Develop a numerical integration program for engineering applications.
3	Develop a polynomial curve fitting program for experimental data.
4	Design a numerical differentiation program and compare results with analytical solutions.
5	Develop a matrix-based application for solving electrical network equations.
6	Design a signal denoising application using basic filtering techniques.

Proposed Assessment Plan for 50 marks:

Tool	Remarks	Marks
Assessment method	Continuous Evaluation Record writing Lab CIE	10 20 20
Total		**50**

Teaching-Learning–Evaluation Scheme:

Sl. No	Teaching and Learning Method	No. of Hours/Week	No. of Weeks	Hours/ Semester
1	Lab Conduction	2	14	28
2	Evaluation	-	-	02
Total Learning Hours/Semester				30

Textbook:

Sl.No	Book Title	Authors	Edition	Publisher	Year
1.	GNU Octave Manual	J. W. Eaton, D. Bateman, S. Hauberg, and R. Wehbring	8th	Boston, MA, USA: Free Software Foundation	2024

Reference books/Manuals:

1. H.Moore,MATLAB for Engineers,5th ed. Upper Saddle River, NJ, USA: Pearson Education, 2018.
2. S.Attaway, MATLAB: A Practical Introduction to Programming and Problem Solving, 5th ed. Oxford, U.K.: Butterworth-Heinemann, 2021.

Weblinks and Video Lectures(e-Resources):

1. Octave Tutorial / Matlab Introduction to Octave: https://www.youtube.com/watch?v=q44zkMy3TWg&list=PLHQqy6aejPhjRPiHEPpxyeSwYfLnbI-lE
2. MATLAB On ramp–MathWorks https://matlabacademy.mathworks.com/details/matlab-onramp/gettingstarted
3. MATLAB Tutorials – Tutorials Point https://www.tutorialspoint.com/matlab/index.htm
4. Signal Processing with MATLAB – MathWorks Examples https://in.mathworks.com/help/signal/examples.html

Course Articulation Matrix

Course Outcomes	Program Outcomes												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**
CO1	3	2	-	1	3	-	-	2	1	-	1	2	2
CO2	3	2	2	2	3	-	-	2	1	-	1	2	2
CO3	2	2	2	2	3	-	-	2	3	-	1	2	2

Semester: III						
PHYSICAL EDUCATION (SPORTS & ATHLETICS)–I						
Course Code	**:**	25PE1		**CIE**	**:**	**100 Marks**
Credits: L:T:P	**:**	0:0:1				
Total Hours	**:**	15 P				

Course Outcomes: At the end of the course, the student will be able to

1. Understand the fundamental concepts and skills of Physical Education, Health, Nutrition and Fitness
2. Familiarization of health-related Exercises, Sports for overall growth and development
3. Create a foundation for the professionals in Physical Education and Sports
4. Participate in the competition at regional/state/national/international levels.
5. Create consciousness among the students on Health, Fitness and Wellness in developing and maintaining a healthy lifestyle.
6. Understand and practice of Traditional Games

Module I: Orientation **4 Hours**

A. Lifestyle
B. Health &Wellness
C. Pre-Fitness test.

Module II: General Fitness & Components of Fitness **4 Hours**

A. Warming up (Free Hand exercises)
B. Strength–Push-up/Pull-ups
C. Speed– 30Mtr Dash

Module III: Specific games (Any one to be selected by the student) **16 Hours**

1. Kabaddi–Handtouch,Toe Touch,Thigh Hold, Anklehold and Bonus.
2. Kho-Kho– Giving Kho, Single Chain, Pole dive, Pole turning, 3-6 Up.

Scheme and Assessment for auditing the course and Grades:

Sl.No.	Activity	Marks
1.	Participation of student in all the modules	20
2.	Quizzes/Assignment–2,eachof 20marks	40
3.	Final presentation/exhibition/Participation In competitions/practical on specific tasks assigned to the students	40
	Total	**100**

Semester III			
Yoga - I			
Course Code	25YOG1	**CIE**	100 Marks
Course Type	NCMC		
Total Hours	2 hrs/week		

Course Objectives

The objectives of this course are to:

1. Introduce students to the origin, history, philosophy, and fundamental concepts of Yoga.
2. Familiarize students with the different schools of Yoga, its aims, objectives, and the importance of prayer in Yogic practice.
3. Develop awareness of the rules, regulations, and safety precautions to be followed during Yogic practices.
4. Enable students to learn and practice Suryanamaskara and selected Yogasanas with proper techniques for improving physical and mental well-being.
5. Promote a healthy life style by encouraging regular Yogic practice, correcting misconceptions about Yoga, and fostering positive health, self-discipline, and overall wellness.

Introduction of Yoga: Yoga, its origin, history and development. Yoga, its meaning, definitions. Different schools of yoga, Aim and Objectives of yoga, **Prayer** : importance of prayer
Brief introduction of yogic practices for common man to promote positive health, **Rules and regulations**: Rules to be followed during yogic practices by practitioner
Suryanamaskara:Suryanamaskar prayer and its meaning, Need, importance and benefits of Suryanamaskar 12 count, 2rounds, Misconceptions of yoga: **Yoga its misconceptions**, Difference between yogic and non yogic practices
Different types of Asanas: Asana, Need, importance of Asana. Different types of asana. Asana its meaning by name, technique, precautionary measures and benefits of each asana, Sitting 1.Padmasana, 2.Vajrasana, Standing 1.Vrikshana, 2.Trikonasana, Proneline1.Bhujangasana, 2.Shalabhasana, Supineline 1.Utthitadvipadasana, 2.Ardhahalasana

Course Outcomes:

Upon successful completion of this course, the student will be able to:

1. Explain the origin, history, philosophy, objectives, and different schools of Yoga, along with its role in promoting holistic health and well-being.
2. Understand and apply the rules, regulations, and ethical practices associated with Yogic exercises, including the significance of prayer and Suryanamaskara.
3. Demonstrate the correct techniques of selected Yogasanas, such as sitting, standing, prone, and supine postures, while observing appropriate precautions.
4. Analyze the physical, mental, and therapeutic benefits of Yogic practices and distinguish between authentic Yogic practices and common misconceptions about Yoga.
5. Adopt Yoga as a regular life style practice to enhance physical fitness, mental wellness, discipline, and overall quality of life.

Suggested Learning Resources: (TextBook/ReferenceBook/Manuals):

Text books:

1. George Feuerstein: the yoga Tradition (its history, literature, philosophy and practice)
2. Sri Ananda: The complete Book of yoga Harmony of Body and Mind (Orient paper Backs: Vision Books Pvt.Ltd..1982.
3. B.K.Slyenkar: Light on the Yoga sutras of Patanjali (Haper Collins Publications India Pvt.Ltd.New Delhi.)
4. Science of Divinity and Realization of Self Vethathiri Publication,(6-11)WCSC,Erode

Reference books/Manuals:

1. Principles and Practice of Yoga in Health Care,Publisher:Handspring Publishing Limited. ISBN:9781909141209,978190914209
2. BasavaraddiIV: Yoga in School Health, MDNIY NewDelhi. 2009
3. Dr.HR.Nagendra: Yoga Research and application (Vivekanda Kendra Yoga Prakashana Bengalore)
4. Dr.Shirley Telles: Glimpses of Human Body (Vivekanda KendraYoga Prakashana Bengalore).

Web links and Video Lectures (e-Resources):

Search by topics to get the videos

Assessment Structure:

This course is having only **Continuous Internal Assessment** (CIE) marks of 100.

Weightage	**Marks**
Attendance to all the sessions	20Marks
Practical sessions on Yoga and Its Benefits	40Marks
Two Assignments	40Marks
Total Marks	100

A student shall obtain a minimum of 40% marks or 40 marks out of 100 to qualify in the course.

Course Title	Community Project / Societal Project		
Course Code	25SCR	(L-T-P)C	(0-0-2)1
Exam	3 Hrs.	Hours/Week	2
CIE + SEE	50 marks + 50 Marks	Total Hours	30

Course Objective: Rapid urbanization, population growth, environmental concerns, energy demand, water scarcity, waste management, transportation issues and rural development challenges have created practical problems affecting communities and public welfare. This course aims to integrate technical knowledge, field exposure and societal engagement so that students identify real community issues, frame problem statements and attempt appropriate, feasible and sustainable engineering responses within the scope of a one-semester project.

Course Outcomes: At the end of the course, the student will be able to:

#	Course Outcomes	Mapping to PO's	Mapping to PSO's
1	Identify and analyze societal problems through field interaction and technical assessment.	1,2,3,4,6,9	-
2	Develop skills in project planning, field survey, data collection, implementation, documentation and reporting.	1,2,3,4,5,8,9,10	-
3	Formulate feasible engineering problem statements and solutions considering practical constraints and sustainability aspects.	1,2,3,5,6,7,10	-
4	Apply principles of environmental responsibility, ethics and societal welfare in engineering practice through community-oriented interventions.	6, 7	-
5	Exhibit multidisciplinary learning and problem-solving ability based on collected data, user feedback and baseline conditions.	2,3,4,5,8,9,11	-
6	Demonstrate teamwork and communication skills while interacting with technical and non-technical stakeholders and reflect on project impact on society.	6,8,9,10,11	-

Restrictions and professional conduct:

Community / Societal Projects shall remain **academic, socially responsible, technically focused, and politically neutra**l. Students and faculty shall maintain professionalism, ethical conduct, public respect and institutional integrity while interacting with communities, public groups, organizations and stakeholders. Students and faculty shall avoid the following during project execution:

- Association with political party activities, campaigns or propaganda.
- Participation in activities that may disturb communal harmony, public order or institutional reputation.
- Use of the project platform for personal, political, ideological or commercial promotion.
- Disrespectful, discriminatory or unethical interaction with community members or stakeholders.

Projects must also recognize constraints related to cost, resources, environment and safety, and stakeholder

behavior/cooperation/acceptance when planning and implementing activities.

SET OF PROJECT ACTIVITIES (TW/SL = 30 HOURS)

Methods for Project Identification:

Students may identify the project topic using one or more of the following methods:

- Interaction with local rural or urban stakeholders such as local leaders, corporation/municipality personnel, NGOs, panchayat representatives, etc.
- Review of issues highlighted in print and electronic media, and social networks (WhatsApp, Facebook, X, Instagram, etc.).
- After selecting a broad topic, students shall collect data, conduct a feasibility survey, estimate timelines and resources, approximate expenditure, and then define the problem statement and objectives clearly.

List of Project Topics and Engineering Outcomes:

The following structured sequence of activities is to be carried out during the semester:

Sl.No	Project Title	Measurable Engineering Outcome	Mapped POs	SDGs
1.	Rural and urban water conservation and management systems	Prepare a site-specific water-saving plan, estimate water demand–supply gap, and propose a feasible conservation intervention with quantified savings.	PO1, PO2, PO3, PO4, PO10, PO11	SDG 6, SDG 11, SDG 12
2.	Waste management and recycling	Conduct waste audit, classify waste streams, and design a segregation/recycling workflow with measurable reduction in mixed waste.	PO2, PO3, PO4, PO6, PO8, PO10	SDG 11, SDG 12, SDG 13
3.	Afforestation	Identify a degraded area, prepare plantation layout, and demonstrate survival-rate tracking and maintenance schedule for saplings.	PO2, PO3, PO4, PO6, PO7, PO11	SDG 11, SDG 13, SDG 15
4.	Biogas generation and power generation	Estimate organic waste availability, size a small biogas system, and document expected gas output or energy yield.	PO1, PO2, PO3, PO4, PO5, PO10	SDG 7, SDG 11, SDG 12
5.	DPR for solar power rural plant	Prepare a DPR with load assessment, panel sizing, cost estimate, and projected energy generation and payback.	PO1, PO2, PO3, PO4, PO5, PO10	SDG 7, SDG 9, SDG 11
6.	DPR for electrification of village/tribal community	Map unserved/underserved households, propose electrification layout, and estimate coverage, losses, and implementation cost.	PO1, PO2, PO3, PO4, PO10, PO11	SDG 7, SDG 9, SDG 10

7.	DPR for rural drainage system	Survey drainage bottlenecks, develop a drainage layout, and estimate runoff handling capacity and flood-risk reduction.	PO1, PO2, PO3, PO4, PO6, PO10	SDG 6, SDG 9, SDG 11
8.	Sustainability and environmental health projects	Assess local environmental health issues and propose interventions with measurable improvement in hygiene, safety, or resource use.	PO2, PO3, PO4, PO6, PO7, PO8	SDG 3, SDG 6, SDG 11, SDG 12
9.	Plastic free campaigns	Measure plastic usage before and after awareness intervention and report percentage reduction or behavioural change.	PO2, PO3, PO6, PO7, PO8, PO10	SDG 11, SDG 12, SDG 13
10.	Health and nutrition awareness	Conduct baseline and post-program awareness survey and document improvement in awareness score or adoption of healthier practices.	PO2, PO6, PO7, PO8, PO9, PO10	SDG 2, SDG 3, SDG 11
11.	Societal projects involving health wellness	Identify a community health need and develop an awareness/service module with measurable participation and feedback outcomes.	PO2, PO3, PO6, PO8, PO9, PO10	SDG 3, SDG 11, SDG 17
12.	Air quality monitoring system	Collect air-quality data, compare with reference limits, and present trends along with possible mitigation suggestions.	PO2, PO3, PO4, PO5, PO6, PO10	SDG 3, SDG 11, SDG 13
13.	Plastic waste reduction campaign	Track collection, segregation, and replacement actions, and quantify reduction in plastic waste generation or littering.	PO2, PO3, PO6, PO7, PO8, PO10	SDG 11, SDG 12, SDG 13
14.	Urban greening projects	Prepare greening plan, identify planting locations, and assess environmental benefits such as shade, aesthetics, or heat mitigation.	PO2, PO3, PO4, PO6, PO7, PO11	SDG 11, SDG 13, SDG 15
15.	Smart agriculture solution	Design a low-cost monitoring or irrigation support solution and estimate improvement in water use efficiency or crop support.	PO1, PO2, PO3, PO4, PO5, PO10	SDG 2, SDG 6, SDG 9
16.	Smart irrigation system	Estimate crop water requirement, propose control logic, and quantify water savings compared with conventional irrigation.	PO1, PO2, PO3, PO4, PO5, PO10	SDG 2, SDG 6, SDG 12
17.	Youth mentoring programmes	Deliver a structured mentoring activity and measure participation, engagement, and skill/awareness improvement.	PO6, PO8, PO9, PO10, PO11	SDG 4, SDG 10, SDG 17
18.	Adult education	Conduct learner-needs assessment, prepare instructional content, and measure improvement in basic literacy	PO6, PO8, PO9, PO10, PO11	SDG 4, SDG 10, SDG 17

		or numeracy indicators.		
19.	Food security initiatives / cold storage system	Estimate storage need, design a simple cold-chain concept, and document reduction in spoilage or wastage.	PO1, PO2, PO3, PO4, PO5, PO10	SDG 2, SDG 9, SDG 12
20.	Human rights awareness with legal systems	Prepare and deliver an awareness module and assess increase in legal awareness and access-to-rights understanding.	PO6, PO7, PO8, PO9, PO10	SDG 5, SDG 10, SDG 16
21.	House tax collection through digital media	Develop a simple digital workflow or awareness support and measure improvement in compliance, convenience, or response time.	PO2, PO3, PO4, PO5, PO10, PO11	SDG 9, SDG 11, SDG 16
22.	Use of application / application program	Build or demonstrate a useful community app and measure usability, adoption, or efficiency improvement.	PO1, PO3, PO4, PO5, PO9, PO10	SDG 9, SDG 11, SDG 17
23.	Creation of Panchayat library	Plan the library model, catalogue resources, and measure usage, accessibility, or participation outcomes.	PO6, PO8, PO9, PO10, PO11 SDG 4,	SDG 10, SDG 11, SDG 17

Prescribed Text Books:

Sl.No	Book Title	Authors	Edition	Publisher
1	Community Engagement and Social Innovation	Phadke, N. D.	1st	Oxford University Press, New Delhi.
2	Project-Based Learning in Engineering Education	Garg, N. R.	1st	Pearson India Education Services, Noida.
3	Service Learning and Community Projects.	Gupta, A. and P. Singh.	1st	McGraw-Hill Education (India), New Delhi.
4	Practical Guide to Community Development Projects	Wilson, G.	2nd	Routledge, London.

Reference Books:

1. NPTEL courses on Project-Based Learning and Social Innovation.
2. SWAYAM courses on community engagement and sustainability.
3. UN Sustainable Development Goals portal: https://sdgs.un.org
4. MyGov India and local civic body portals for community initiatives.
5. YouTube resources on design thinking, social innovation, and community service learning.

6. NGO and government field-action case studies related to sanitation, water, health, education, and environment.

Web links and Video Lectures (e-Resources):

1. NPTEL courses on Engineering Geology (IIT Roorkee, IIT Kharagpur).
2. NPTEL courses on Soil Mechanics and Foundation Engineering (IIT Delhi, IIT Bombay).
3. Virtual Labs – Geotechnical Engineering Virtual Lab (IIT Kanpur): https://vlab.co.in
4. Geological Survey of India (GSI) – Maps, reports, and publications: https://www.gsi.gov.in
5. YouTube channels: Civil Engineering Essentials, The Engineering Classroom (soil mechanics experiments).
6. American Society of Civil Engineers (ASCE) – Geotechnical resources and standards

Teaching-Learning Process:

Week / Phase	Teaching-Learning Activity	Faculty Role	Student Activity	Output / Evidence
1	Course introduction, objectives, ethics, conduct, and assessment briefing	Explain course scope, rules, rubrics, and expected deliverables	Understand course requirements and form teams	Team list, course plan
2	Community problem identification and topic selection	Guide topic framing and feasibility	Identify local issues through discussion and observation	Shortlisted project topic
3	Stakeholder interaction and preliminary survey	Demonstrate survey methods and stakeholder engagement	Collect initial data from community/users	Survey notes, interview record
4	Problem statement and objective formulation	Review and refine problem statement	Prepare problem statement, scope, and objectives	Approved problem statement
5	Literature/case study review and baseline analysis	Suggest relevant references and examples	Study existing solutions and compare approaches	Baseline analysis summary
6	Project planning and role assignment	Help teams organize tasks, timeline, and	Plan activities, divide roles, and	Work plan / Gantt chart

		responsibilities	prepare schedule	
7	Feasibility analysis and solution brainstorming	Check technical feasibility and practicality	Generate possible engineering solutions	Solution alternatives sheet
8	Selection of final solution and design approach	Review final concept and design logic	Finalize concept, methods, and expected outcome	Concept note / design outline
9	Data processing / calculations / sizing / mapping	Support computations and technical review	Analyze data, perform calculations, prepare maps/charts	Technical analysis sheet
10	Prototype / model / audit / DPR / app development	Monitor progress and correct technical issues	Develop the selected output	Working model / draft DPR / map / app
11	Testing, refinement, and implementation planning	Evaluate technical correctness and improvements	Test prototype or validate proposal with users	Test results / revised output
12	Field implementation / demonstration / awareness activity	Facilitate community interaction and documentation	Conduct implementation or demonstration	Photos, attendance, implementation record
13	Documentation of outcomes, feedback, and impact	Review report structure and completeness	Compile findings, stakeholder feedback, and observations	Draft report
14	Presentation preparation and viva practice	Conduct mock presentation and feedback	Prepare slides/poster and rehearse	Presentation deck
15	Final presentation, submission, and reflection	Evaluate performance using rubrics	Present project, submit report, reflect on learning	Final report, presentation, viva

Assessment structure:

A. Continuous Internal Evaluation (CIE) – 50 marks

• Students, in batches of 3–4, shall undertake at least one project (or a combination of two related activities) aiming, as far as possible, at a logical implemented or implementable outcome.

• CIE will be conducted by a departmental committee (HoD/nominee, guide and one senior faculty) using the following rubrics totaling 50 marks:

B. Semester End Examination (SEE) – 50 marks

• The SEE shall be conducted batch-wise by a committee of : one faculty from the same department and one from a different department.

CIE and SEE Rubrics

Criterion	Weight (marks)	Excellent (Full marks)	Good	Fair	Needs Improvement
Problem identification & Relevance to society/industry/community	8	Problem is clearly identified with strong evidence of societal relevance and well-defined scope.	Problem is relevant and scope is clear with adequate supporting evidence.	Problem defined but justification or evidence is weak.	Problem unclear or not relevant; little/no supporting evidence.
Formation of problem statement; Engineering approach, innovation & feasibility	10	Problem statement is precise; approach is sound, innovative and clearly feasible.	Problem statement adequate; approach feasible with minor gaps.	Problem statement partial; approach feasibility is marginal.	Problem statement missing or approach not feasible.
Interaction with stakeholders; Data collection, analysis & interpretation	8	Thorough stakeholder engagement; data collection is comprehensive; analysis is well-interpreted.	Good engagement; data analysis adequate with minor gaps.	Limited engagement; data incomplete and analysis superficial.	Little/no stakeholder contact; insufficient or no data/analysis.
Project documentation; Clarity, organization & problem-solving demonstrated	10	Documentation is complete, well-organized, analytical, and shows strong problem-solving.	Documentation complete and clear with some analytical content.	Documentation on basic with omissions; problem-solving limited.	Documentation missing/poorly organized; no clear problem-solving.
Communication & Presentation skills	6	Presentation is confident, structured, and answers queries	Presentation clear and satisfactory; responds to	Presentation acceptable but lacks clarity or confidence;	Presentation poor or absent; unable to respond.

		fully; visuals effective.	most queries.	weak responses.	
Contribution & Benefit to society (impact, sustainability)	8	Clear, demonstrable societal benefit and sustainability; realistic path to implementation.	Benefit plausible; sustainability considered with minor gaps.	Limited or unclear societal benefit; sustainability not well addressed.	No evident benefit or sustainability; project not community-oriented.

Course Title	Programmable Logic Devices and FPGA		
Course Code	25VL401	(L-T-P) C	(3-0-0)3
Exam	3Hours	Hours/Week	03
SEE	50Marks	Total Hours	42L + 48ABL = 90

Course Objective: To develop an understanding of programmable logic devices, FPGA architecture, and their applications in digital system design. To provide knowledge of advanced digital design techniques, state machines, microprogramming, floating-point arithmetic, and FPGA-based implementation.

Course Outcomes: with mapping shown against the Program Outcomes (POs)
Upon completion of the course, students shall be able to:

CO's	Course Outcomes	Mapping to POs	Mapping to PSOs
1.	Identify and differentiate various Programmable Logic Devices (PLDs), CPLDs, and FPGAs for digital system design.	1, 2, 5, 11	1, 2
2.	Design combinational and sequential digital systems using advanced digital design techniques and state machine charts.	1, 2, 3, 4, 5, 8, 11	1, 2
3.	Apply microprogramming, floating-point arithmetic, and simulation primitives in digital system implementation.	1, 2, 3, 4, 5, 8, 9, 11	1, 2
4.	Implement and evaluate digital functions using FPGA logic blocks, carry chains, cascade chains, and dedicated multipliers.	1, 2, 3, 4, 5, 8, 9, 11	1, 2

Course Contents:

Module1	10 Hours

Introduction to Programmable Logic Devices and Digital Design: Hazards in Combinational Circuits, Brief Overview of Programmable Logic Devices, Simple Programmable Logic Devices (SPLDs), Complex Programmable Logic Devices (CPLDs), Field-Programmable Gate Arrays (FPGAs), BCD to 7-Segment Display Decoder, BCD Adder, Traffic Light Controller, Synchronization and Debouncing.

Module2	11 Hours

Advanced Digital Design and SM Charts: Shift-and-Add Multiplier, Array Multiplier, Signed Integer/Fraction Multiplier (Excluding Test Bench), Keypad Scanner, State Machine Charts, Derivation of SM Charts, SM Chart for Binary Multiplier, Dice Game (Excluding Test Bench), Realization of SM Charts, Implementation of the Dice Game.

Module3	11 Hours

Microprogramming and Floating-Point Arithmetic: Microprogramming, Linked State Machines, Representation of Floating-Point Numbers, Floating-Point Multiplication, Floating-Point Addition, Other Floating-Point Operations, Multivalued Logic and Signal Resolution, Built-in Primitives, User-Defined Primitives, SRAM Model, Rise and Fall Delays of Gates.

MODULE-4	10 Hours

Designing with Field-Programmable Gate Arrays: Implementing Functions in FPGAs, Carry Chains in FPGAs, Cascade Chains in FPGAs, Examples of Logic Blocks in Commercial FPGAs, Dedicated Multipliers in FPGAs, FPGA Capacity: Maximum Gates versus Usable Gates, Design Translation.

Prescribed Textbooks:

Sl. No.	Book Title	Authors	Edition	Publisher	Year
1	Digital Systems Design Using Verilog	Charles H. Roth, Jr. Lizy Kurian John Byeong Kil Lee	1st	Cengage Learning	2014
2	Advanced FPGA Design Architecture, Implementation, and Optimization.	Steve Kilts	1st	John Wiley & Sons, Inc., Hoboken, New Jersey.	2007

Reference Books:

Sl. No	Book Title	Authors	Edition	Publisher	Year
1.	Field-Programmable Gate Array Technology	Stephen M. Trimberger	1st	Springer	1994
2.	Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation	Scott Hauck and André DeHon	1st	Morgan Kaufmann	2008
3	FPGA Prototyping by Verilog Examples	Pong P. Chu	2nd	Wiley	2008

Web links and Video Lectures (e-Resources):

1. https://www.youtube.com/watch?v=g95RMz233Jc
2. https://www.amd.com/en/corporate/university-program/adaptive-computing-training.html
3. https://nptel.ac.in/courses/108106177
4. https://www.youtube.com/watch?v=msXKWn24TN4

Teaching-Learning–Evaluation Scheme:

Sl. No	Teaching and Learning Method	No. of Hours/ Week	No. of Weeks	Hours/ Semester
1.	Classroom Teaching &Learning	3	14	42
2.	Activity Based Learning (ABL1&ABL2)	-	-	38
3.	Evaluation of Learning Process	-	-	10
Total Learning Hours/Semester				**90**

Proposed Assessment Plan (for 50 marks of CIE):

Tool	Remarks	Marks
CIE	Two tests conducted for 50 marks each and reduced to 15 marks	30
Activity Details	Details of activities to be conducted **Activity 1: FPGA Architecture and Device Analysis** Students shall study the architecture of a commercially available FPGA device (e.g., Xilinx Artix-7 or AMD Spartan series) and prepare a report highlighting the configurable logic blocks, routing resources, clock management, memory resources, DSP slices, I/O architecture, and typical application areas. **Activity 2: FPGA Design Flow Case Study** Students shall select a digital design (such as a traffic light controller, UART, PWM generator, or vending machine controller) and document the complete FPGA implementation flow, including design specification, synthesis, implementation, timing analysis, resource utilization, and hardware validation using Vivado.	20
Total		**50**

Activity Based Learning (38Hours)

Activity 1		**Hours**
FPGA Architecture and Device Analysis	Study of FPGA architectures	6
	Preparation of report on CLB's routing resources	6
	Preparation of report on Clock management, memory resources, DSP slices.	4
	Documentation of I/O architectures and application areas.	4
Total		**20**
Activity 2		
FPGA Design Flow Case Study	Simulation of digital design	6
	Preparation and planning for simulation activities	6
	Execution and verification of simulation results	2
	Documentation of simulation outcomes	4
Total		**18**

Evaluation of Learning Process (10Hours)

Type of Evaluation	**Hours**
CIE (1 and 2)	3
Demonstration of activity and report submission	4
Semester End Exam	3
Total	**10**

Course Articulation Matrix

Course Outcomes	Program Outcomes												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**
CO1	3	2	-	-	2	-	-	-	-	-	1	3	2
CO2	3	3	3	2	3	-	-	1	-	-	1	3	3
CO3	3	3	2	3	3	-	-	1	1	-	1	3	3
CO4	3	2	3	2	3	-	-	2	1	-	1	3	3

Course Title	Analog Electronics - II		
Course Code	25VL402	(L-T-P) C	(3-0-2)4
Exam	3 hours	Hours/Week	5 hours
SEE	50 marks	Total Hours	42L+28P+50ABL=120

Course Objective: To equip students with the analytical and design skills required to develop differential and operational amplifier circuits, timer-based and active filter circuits, and data conversion systems, using both discrete op-amp applications and CMOS amplifier architectures.

Course outcomes: Upon completion of the course, the student shall be able to:

CO's	Course Outcomes	Mapping to POs	Mapping to PSOs
1.	Analyze the operation and performance of CMOS differential amplifiers and their configurations used in analog integrated circuits.	1, 2, 3, 5,	1
2.	Design and evaluate CMOS operational amplifiers and DC voltage regulator circuits to meet specified performance requirements.	1, 2, 3, 5, 8, 9	1
3.	Apply operational amplifier circuits including voltage followers, inverting/non-inverting amplifiers, summing and difference amplifiers, instrumentation amplifiers, integrators, differentiators, comparators, Schmitt triggers, and precision rectifiers — for signal conditioning and processing applications	1, 2, 3, 5, 8	1
4.	Explain the internal architecture and functional blocks of the 555 timer to design astable and monostable multivibrator circuits, and describe the fundamentals of active filters, DC voltage regulators, and analog-to-digital/digital-to-analog conversion techniques.	1, 2, 5, 8, 9	1

Course Contents:

Module1	10 Hours

Differential Amplifiers: Single ended and differential operation, Basic differential pair, Qualitative Analysis, Quantitative Analysis, Degenerated Differential Pair, Common-mode response, Differential pair with MOS Loads, Gilber Cell. **Text Book1:** 4.1,4.2, 4.3, 4.4, 4.5

Module2	10 Hours

Operational-Amplifier Circuits: The Two-Stage CMOS Op-Amp, The Circuit, Input Common-Mode Range and Output Swing, DC Voltage Gain, Common-Mode Rejection Ratio (CMRR), Frequency Response, Slew Rate, Power-Supply Rejection Ratio (PSRR), The Folded-Cascode CMOS Op-Amp, Input Common-Mode Range and Output Swing, Voltage Gain, Frequency Response, Slew Rate, Increasing the Input Common-Mode Range: Rail-to-Rail Input Operation, BJT Op-Amp Techniques.
Text Book2: 13.1,13.2,13.3

Module3	11 Hours

Operational Amplifier Applications: Applications of Operational Amplifiers: Voltage Follower, Non-Inverting Amplifier, Inverting Amplifier, Summing Amplifier, Difference Amplifier, Instrumentation Amplifier, Differentiator, Integrator, Schmitt Trigger, Comparator, Precision Rectifier.
Text Book3: 3.2, 3.3, 3.4, 3.6,3.7,3.8, 8.3, 8.5, 8.6, 8.7, 9.1,9.2

MODULE-4	11 Hours

555 Timer: Internal Architecture, Functional Blocks, Astable Multivibrator, Monostable Multivibrator, Timer Pulse Generation. **Active Filters**: Filter Types and Characteristics. **DC Voltage Regulators**: Voltage Regulator Basics, **Digital to Analog and Analog to Digital Conversion:** Analog/Digital Conversion Basics, Digital to Analog Conversion. **Text Book3**: 10.1,10.2,10.6, 10.7, 12.1, 13.1, 15.1,15.2, 16.1, 16.2,

Prescribed Textbooks:

Sl. No.	Book Title	Authors	Edition	Publisher	Year
1.	Design of Analog CMOS Integrated Circuits	Behzad Razavi	2nd	McGraw-Hill Education	2017
2.	Microelectronic Circuits, Theory and Applications	Adel S. Sedra Kenneth C. Smith	7th	Oxford university press	2009
3.	Operational Amplifiers and Linear IC's'	David A. Bell	3rd	Oxford University Press 2011	2011

Reference Books:

Sl. No	Book Title	Authors	Edition	Publisher	Year
1.	Fundamentals of Microelectronics	Behzad Razavi	2^{nd}	Wiley India Pvt. Ltd	2014
2.	Electronic Devices and Circuits Theory	Robert L. Boylestad and Louis Nashelsky	10^{th}	Pearson,	2012
3.	Op Amps and Linear Integrated Circuits	Ramakant A Gayakwad	4^{th}	Pearson Education	2015

Weblinks and Video Lectures(e-Resources):

- https://www.nptel.ac.in/courses/108106105
- https://onlinecourses-archive.nptel.ac.in/noc18_ec05/preview
- https://www.youtube.com/@BehzadRazaviElectronics
- https://training.ti.com/ti-precision-labs-op-amps

Teaching-Learning–Evaluation Scheme:

Sl. No	Teaching and Learning Method	No. of Hours/ Week	No. of Weeks	Hours/ Semester
1.	Classroom Teaching & Learning	3	14	42
2.	Evaluation of Learning Process	-	-	10
3.	Integrated Lab (Fixed Experiments)	2	14	28
4.	Integrated Lab (Open-ended Experiments)	-	-	40
Total Learning Hours/Semester				**120**

Proposed Assessment Plan (for 50 marks of CIE):

Tool	Remarks	Marks
CIE	Two CIEs conducted for 50 marks each and reduced to 15 marks	30
Activity Details	Integrated lab experiments (Open-ended experiments)	20

Integrated lab experiments

Sl. No.	PART-A: Fixed Experiments
1	**Design and Simulation of CMOS Differential Pair**- Analyze differential-mode and common-mode operation, differential gain, common-mode gain, and CMRR.
2	**Simulation of CMOS Differential Amplifier Configurations**- Compare resistive load, active load, and current mirror load
3	**Design and Simulation of CMOS Operational Amplifiers**- Analyze the performance of single-stage CMOS operational amplifiers.
4	**Design and Simulation of CMOS Operational Amplifiers**- Analyze the performance of two-stage CMOS operational amplifiers.
5	**Design and Simulation of DC Voltage Regulators**- Simulate series, shunt, and op-amp-based voltage regulators and evaluate line and load regulation.
6	**Simulation of Op-Amp Linear Applications**- Implement voltage follower, inverting amplifier, non-inverting amplifier, summing amplifier, and difference amplifier.
7	**Simulation of Op-Amp Signal Conditioning Circuits**- Implement integrator, differentiator.
8	**Design and Simulation of Active Filters**- Design first-order low-pass and high-pass active filters and analyze frequency response.
9	**Simulation of 555 Timer Circuits**- Implement Astable multivibrator and analyze pulse generation.
10	**Simulation of 555 Timer Circuits**- Implement monostable multivibrator and analyze pulse generation.
Sl. No.	**PART-B: Open-ended Experiments**
1	**Design a CMOS Differential Amplifier**- Design a differential amplifier to achieve a specified differential gain, CMRR, and output swing.
2	**Design a Two-Stage CMOS Operational Amplifier**- Design an operational amplifier to meet specified gain, bandwidth, phase margin, and slew rate requirements.
3	**Design a Precision Voltage Regulator**- Design an op-amp-based voltage regulator with specified output voltage, line regulation, and load regulation.
4	**Design an Instrumentation Amplifier**- Develop an instrumentation amplifier for low-level sensor signal conditioning with high CMRR.
5	**Design an Active Filter**- Design a low-pass, high-pass, band-pass, or band-stop filter for a specified cutoff frequency.
6	**Design a 555 Timer Application**- Design a timer-based application such as a pulse generator, PWM generator, LED flasher, or time-delay controller.

Course Articulation Matrix:

Course Outcomes	Program Outcomes												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO 2**
CO1	3	3	1	1	2	-	-	-	-	-	-	3	-
CO2	3	3	3	2	3	-	-	2	1	-	-	3	-
CO3	3	2	3	2	3	-	-	2	1	-	-	3	-
CO4	3	3	3	3	3	-	-	2	2	-	-	3	-

Course Title	Network Analysis		
Course Code	25VL403	(L-T-P) C	(3-0-0) 3
Exam	3 Hours	Hours/Week	03
SEE	50 Marks	Total Hours	42L+48ABL=90

Course Objective: To provide students with a strong foundation in electrical network analysis using fundamental circuit laws, network theorems, and analytical techniques. The course enables students to analyze linear electrical networks using Laplace transforms, two-port network parameters, and resonance concepts.

Course Outcomes: with mapping shown against the Program Outcomes (POs)
Upon completion of the course, students shall be able to:

CO's	Course Outcomes	Mapping to POs	Mapping to PSOs
1.	Apply fundamental circuit analysis techniques, including source transformation, mesh analysis, and nodal analysis, to solve DC and AC electrical networks.	1, 2, 3, 5,	1
2.	Analyze electrical networks using network theorems such as Superposition, Thevenin's, Norton's, Maximum Power Transfer, and Millman's theorem.	1, 2, 3, 4, 5	1
3.	Evaluate the transient and steady-state response of RL, RC, and RLC circuits using initial conditions and Laplace transform techniques.	1, 2, 3, 4, 5, 11	1
4.	Analyze two-port networks using parameter models and evaluate the resonance characteristics of electrical circuits in terms of frequency response, quality factor, and bandwidth.	1, 2, 3, 4, 5	1

Course Contents:

Module1	10 Hours

Basic Concepts: Types of sources, Star delta transformation, mesh and nodal analysis with linearly dependent and independent sources for DC and AC networks, source transformations.

Module2	10 Hours

Network Theorems: Superposition theorem, Thevenin's theorem, Norton's Theorem, Maximum power transfer theorem, Millman's theorem, Problems.

Module3	11 Hours

Initial Conditions & Laplace transform: Behaviour of circuit elements under switching condition and their Representation, evaluation of initial and final conditions in RL, RC and RLC circuits.

Laplace Transform: step, ramp responses, Solution of networks, Laplace transform of waveform

MODULE-4	11 Hours

Two Port Network Parameters: Definition of Z, Y, h and Transmission parameters, modeling with these parameters, relationship between parameters sets. Concepts of reciprocity two port networks.

Resonance: Series and parallel resonance- Frequency- response, Quality Factor, Bandwidth of Series and Parallel circuits.

Prescribed Textbooks:

Sl. No.	Book Title	Authors	Edition	Publisher	Year
1	Networks and systems	Roy Choudhury	2nd	New Age International Publications	2013
2	Network analysis	VanValkenberg	3rd	Prentice Hall of India	2019

Reference Books:

Sl. No	Book Title	Authors	Edition	Publisher	Year
1.	Engineering Circuit Analysis	Hayt, Kemmerlyand Durbin	7th	TMH	2010
2.	Fundamentals of Electric Circuits	Charles K Alexander and Mathew NO Sadiku	3rd	TMH	2009

Web links and Video Lectures (e-Resources):

1. https://nptel.ac.in/courses/108105159

Teaching-Learning–Evaluation Scheme:

Sl. No	Teaching and Learning Method	No. of Hours/ Week	No. of Weeks	Hours/ Semester
1.	Classroom Teaching &Learning	3	14	42
2.	Activity Based Learning (ABL1&ABL2)	-	-	38
3.	Evaluation of Learning Process	-	-	10
Total Learning Hours/Semester				**90**

Proposed Assessment Plan (for 50 marks of CIE):

Tool	Remarks	Marks
CIE	Two tests conducted for 50 marks each and reduced to 15 marks	30
Activity Details	Details of activities to be conducted **Activity 1: Circuit Simulation Using SPICE:** Analyze DC, AC, and transient responses of RL, RC, and RLC circuits using simulation tools such as LTspice, Ngspice, or Multisim, and compare the results with theoretical calculations. **Activity 2: Network Theorem Verification:** Verify Thevenin's, Norton's, Superposition, and Maximum Power Transfer theorems by solving selected circuits analytically and validating the results through simulation or laboratory experiments.	20
Total		**50**

Activity Based Learning (38Hours)

Activity 1		**Hours**
Circuit Simulation Using SPICE	Analysis of DC, AC, and transient responses of RL, RC, and RLC circuits using LTspice, Ngspice, or Multisim	6
	Preparation and planning of simulation studies and comparison with theoretical calculations	6
	Execution and verification of simulation results	4
	Documentation of simulation observations and performance analysis	4
Total		**20**
Activity 2		
Network Theorem Verification	Analytical verification of Thevenin's, Norton's, Superposition, and Maximum Power Transfer theorems	6
	Simulation or laboratory validation of network theorems	6
	Comparison and verification of analytical and simulation results	2
	Documentation of observations, conclusions, and report preparation	4
Total		**18**

Evaluation of Learning Process (10Hours)

Type of Evaluation	**Hours**
CIE (1 and 2)	3
Demonstration of activity and report submission	4
Semester End Exam	3
Total	**10**

Course Articulation Matrix

Course Outcomes	**Program Outcomes**												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**
CO1	3	3	1	-	2	-	-	-	-	-	-	2	-
CO2	3	3	2	1	2	-	-	-	-	-	-	2	-
CO3	3	3	2	2	2	-	-	-	-	-	1	2	-
CO4	3	3	2	2	3	-	-	1	1	-	-	2	-

Course Title	Computer Organization and ARM Processor		
Course Code	25VL404	(L-T-P) C	(3-0-0)3
Exam	3Hours	Hours/Week	03
SEE	50Marks	Total Hours	42L + 48ABL = 90

Course Objective: To provide students with a strong foundation in computer organization, processor architecture, memory hierarchy, and input/output systems. The course introduces ARM architecture and instruction set, enabling students to understand the design and operation of modern embedded computing systems.

Course Outcomes: with mapping shown against the Program Outcomes (POs)
Upon completion of the course, students shall be able to:

CO's	Course Outcomes	Mapping to POs	Mapping to PSOs
1	Describe the basic organization of computer systems, instruction formats, addressing modes, and memory organization.	1, 2, 5	1
2	Analyze processor organization, memory hierarchy, cache memory, DMA, and input/output operations in computer systems.	1, 2, 3, 4, 5	1
3	Explain the architecture, design philosophy, processor organization, and hardware components of ARM-based embedded systems.	1, 2, 3, 4, 5, 8, 9	1
4	Apply ARM instruction sets and assembly language programming concepts to develop simple embedded system applications.	1, 2, 3, 4, 5, 8, 9, 11	1

Course Contents:

Module1	10 Hours

Basic Structure of Computers: Functional Units, Basic Operational Concepts, Bus Structure, Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement.
Machine Instructions and Programs: Memory Locations and Addresses, Memory Operations, Instruction and Instruction Sequencing, Addressing Modes, Assembly Language Directives.
Textbook-1: Chapters **1.2, 1.3, 1.4, 1.6, 2.2, 2.3, 2.4, 2.5, 2.6.1**

Module2	10 Hours

Input/Output Organization: Accessing I/O Devices, Programmed I/O, Interrupts, Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Direct Memory Access (DMA).
Memory Organization: Bus Arbitration, Memory Hierarchy, Cache Memories, Cache Mapping Techniques, Performance Considerations.
Textbook-1: Chapters **4.1, 4.2, 4.2.1, 4.2.2, 4.2.3, 4.4, 5.4, 5.5.1**

Module3	11 Hours

Processor Organization: Register Transfers, ALU Operations, Instruction Cycle, Instruction Execution, Control Unit Fundamentals.
Pipelining: Basic Concepts, Pipeline Hazards, Performance Improvement, Role of Cache Memory.
ARM Embedded Systems: Introduction, RISC Design Philosophy, ARM Architecture Overview, AMBA Bus Protocol, ARM Memory Organization, Peripherals, Embedded Software, Boot Process, Operating System and Applications.
Textbook-1: Chapters **7.1, 7.2, 8.1**
Textbook-2: Chapters **1.1–1.5**

MODULE-4	11 Hours

ARM Processor and Instruction Set: ARM Core Data Flow Model, Registers, Current Program Status Register (CPSR), Pipeline, Exceptions, Interrupts and Vector Table, Core Extensions.
ARM Instruction Set: Data Processing Instructions, Load–Store Instructions, Branch Instructions, Program Status Register Instructions, Software Interrupt Instructions, Loading Constants, ARMv5E Extensions, Conditional Execution. **Textbook-2:** Chapters **2.1–2.5, 3.1–3.9**

Prescribed Textbooks:

Sl. No.	Book Title	Authors	Edition	Publisher	Year
1	Computer Organization	Carl Hamacher, Zvonko Vranesic, Safwat Zaky	5th	Tata McGraw-Hill	2002
2	ARM System Developer's Guide	Andrew N. Sloss, Dominic Symes, Chris Wright	1st	Morgan Kaufmann (Elsevier)	2008

Reference Books:

Sl. No	Book Title	Authors	Edition	Publisher	Year
1.	Computer Organization and Architecture	William Stallings	9th	Pearson	2013
2.	Computer Organization and Design: The Hardware/Software Interface – ARM	David A. Patterson and John L. Hennessy	4th	Elsevier	2010

Web links and Video Lectures (e-Resources):

1. https://nptel.ac.in/courses/106106092
2. https://nptel.ac.in/courses/106106166
3. https://nptel.ac.in/courses/106103180
4. https://nptel.ac.in/courses/108105102

Teaching-Learning–Evaluation Scheme:

Sl. No	Teaching and Learning Method	No. of Hours/ Week	No. of Weeks	Hours/ Semester
1.	Classroom Teaching &Learning	3	14	42
2.	Activity Based Learning (ABL1&ABL2)	-	-	38
3.	Evaluation of Learning Process	-	-	10
Total Learning Hours/Semester				**90**

Proposed Assessment Plan (for 50 marks of CIE):

Tool	Remarks	Marks
CIE	Two tests conducted for 50 marks each and reduced to 15 marks	30
Activity Details	**Activity 1: ARM Assembly Programming** Write and simulate simple ARM assembly language programs (e.g., arithmetic operations, data transfer, looping, conditional branching) using an ARM simulator such as Keil µVision or ARM DS. Analyze the execution flow and register contents.	

	Activity 2: Processor and Memory Organization Case Study Conduct a case study on the architecture of a modern ARM-based embedded processor (e.g., Cortex-M or Cortex-A). Prepare a report highlighting the processor organization, memory hierarchy, cache, I/O interfaces, and embedded applications, followed by a seminar presentation.	20
Total		**50**

Activity Based Learning (38Hours)

Activity 1		**Hours**
ARM Assembly Programming	Development and simulation of ARM assembly language programs for arithmetic operations, data transfer, looping, and conditional branching using Keil µVision or ARM DS	6
	Preparation and planning of assembly program development and simulation activities	6
	Execution, debugging, and verification of program execution flow and register contents	4
	Documentation of program outputs, execution analysis, and observations	4
Total		**20**
Activity 2		
Processor and Memory Organization Case Study	Study of ARM-based embedded processor architecture (Cortex-M/Cortex-A), processor organization, memory hierarchy, cache, and I/O interfaces	6
	Preparation of a technical report on processor architecture and embedded applications	6
	Seminar presentation and discussion on the selected processor architecture	2
	Documentation of findings, analysis, and conclusions	4
Total		**18**

Evaluation of Learning Process (10Hours)

Type of Evaluation	**Hours**
CIE (1 and 2)	3
Demonstration of activity and report submission	4
Semester End Exam	3
Total	**10**

Course Articulation Matrix

Course Outcomes	Program Outcomes												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**
CO1	3	2	-	-	2	-	-	-	-	-	-	2	-
CO2	3	3	1	1	2	-	-	-	-	-	-	2	-
CO3	3	3	2	2	3	-	-	1	1	-	-	3	-
CO4	3	3	3	2	3	-	-	1	2	-	1	3	-

Course Title	Control Systems		
Course Code	25VL405	(L-T-P) C	(3-0-0) 3
Exam	3 Hrs	Hours/Week	03
SEE	50 Marks	Total Hours	42L+48ABL=90

Course Objective: The course aims to provide students with the fundamental concepts of modeling, analysis, and design of linear feedback control systems using time-domain, frequency-domain, and state-space techniques. It also introduces the application of control system principles in modern electrical, electronics, and analog/mixed-signal VLSI systems.

Course Outcomes: with mapping shown against the Program Outcomes (POs)
Upon completion of the course, students shall be able to:

CO's	Course Outcomes	Mapping to POs	Mapping to PSOs
1.	Model physical systems and obtain transfer functions using block diagram reduction and signal flow graph techniques.	1, 2, 3, 5,	1
2.	Analyze the transient and steady-state response of first- and second-order feedback control systems.	1, 2, 3, 4, 5	1
3.	Determine the stability and relative stability of control systems using Routh criterion, Root Locus, Nyquist criterion, and Bode plots.	1, 2, 3, 4, 5, 8, 9	1
4.	Develop state-space models of linear systems and identify the application of feedback control concepts in analog and mixed-signal VLSI systems.	1, 2, 3, 4, 5, 8, 9, 11	1,2

Course Contents:

Module1	10 Hours

Introduction: Types of Control Systems, Effect of Feedback Systems, Differential equations of Physical Systems – Mechanical Systems, Electrical Systems, Electromechanical Systems, Analogous Systems.
Block Diagrams: Transfer functions, Block diagram algebra.

Module2	10 Hours

Signal Flow Graphs: Signal Flow Graphs, Mason's Gain Formula (State variable formulation excluded), Signal Flow Graphs for block diagrams, electrical networks and algebraic equations.
Time Response of Feedback Control Systems & Stability Analysis: Standard test signals, Unit step response of first and second order systems, Time response specifications, Steady-state errors and error constants, Effect of feedback on system performance, Disturbance and noise rejection.

Module3	11 Hours

Concepts of Stability: Necessary conditions for Stability, Routh Stability Criterion.
Root-Locus Techniques: Introduction, Root Locus concepts, Construction of Root Loci, Effect of pole-zero locations on system response.
Stability in the Frequency Domain: Mathematical preliminaries, Nyquist Stability Criterion (Inverse polar plots excluded), Assessment of relative stability using Nyquist Criterion (Systems with transportation lag excluded), Gain Margin and Phase Margin.

MODULE-4	11 Hours

Frequency Domain Analysis: Correlation between time and frequency response, Bode Plots, Experimental determination of transfer function, Assessment of relative stability using Bode Plots.
Introduction to State Variable Analysis: Concepts of state, State variables and State models for electrical systems, Solution of state equations.
Applications of Control Systems: Feedback in CMOS/Analog circuits, Basic concepts of frequency compensation, Applications in Phase-Locked Loops (PLLs), Voltage Regulators and Analog/Mixed-Signal VLSI systems.

Prescribed Textbooks:

Sl. No	Book Title	Authors	Edition	Publisher	Year
1	Control Systems Engineering	I J Nagrath, M Gopal	6th	NEW AGE International Publishers	2022
2	Control Systems	Dhanesh. N. Malik	4th	Cengage Learning India Pvt. Ltd	2017

Reference Books:

Sl. No	Book Title	Authors	Edition	Publisher	Year
1	Modern Control Engineering	Katsuhiko Ogata,	5th	Prentice Hall	2015
2	Control Systems Principles and Design	M Gopal	5th	TMH	2012

Web links and Video Lectures (e-Resources):

1. http://docs.znu.ac.ir/members/pirmohamadi_ali/Control/Katsuhiko%20Ogata%20_%20Modern%20Control%20Engineering%205th%20Edition.pdf
2. https://my.ece.utah.edu/~bodson/ifs/control.pdf
3. https://archive.nptel.ac.in/courses/107/106/107106081/
4. https://nptel.ac.in/courses/108106098

Teaching-Learning–Evaluation Scheme:

Sl. No	Teaching and Learning Method	No. of Hours/ Week	No. of Weeks	Hours/ Semester
1.	Classroom Teaching &Learning	3	14	42
2.	Activity Based Learning (ABL1&ABL2)	-	-	38
3.	Evaluation of Learning Process	-	-	10
Total Learning Hours/Semester				**90**

Proposed Assessment Plan (for 50 marks of CIE):

Tool	Remarks	Marks
CIE	Two tests conducted for 50 marks each and reduced to 15 marks	30
Activity Details	Details of activities to be conducted **Activity 1: Simulation-Based Analysis:** Simulate the time response and frequency response of first- and second-order control systems using MATLAB/Simulink, Scilab/Xcos, or Python, and analyze the effect of system parameters on performance and stability. **Activity 2: Case Study on Feedback Control Applications:** Prepare a short report or presentation on the application of feedback	20

	control in engineering systems such as **Phase-Locked Loops (PLLs), voltage regulators, DC motor speed control, or cruise control systems**, highlighting the role of stability and feedback.	
Total		**50**

Activity Based Learning (38Hours)

Activity 1		**Hours**
Simulation-Based Analysis	Simulation of time and frequency responses of first- and second-order control systems using MATLAB/Simulink, Scilab/Xcos, or Python	6
	Preparation and planning of simulation activities for performance and stability analysis	6
	Execution and verification of simulation results by varying system parameters	4
	Documentation of simulation observations, performance characteristics, and conclusions	4
Total		**20**
Activity 2		
Case Study on Feedback Control Applications	Study of feedback control applications such as PLLs, voltage regulators, DC motor speed control, or cruise control systems	6
	Preparation of a technical report highlighting stability, feedback, and system performance	6
	Seminar presentation and discussion on the selected feedback control application	2
	Documentation of findings, analysis, and conclusions	4
Total		**18**

Evaluation of Learning Process (10Hours)

Type of Evaluation	**Hours**
CIE (1 and 2)	3
Demonstration of activity and report submission	4
Semester End Exam	3
Total	**10**

Course Articulation Matrix

Course Outcomes	Program Outcomes												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**
CO1	3	3	1	-	2	-	-	-	-	-	-	2	-
CO2	3	3	2	2	2	-	-	-	-	-	-	2	-
CO3	3	3	2	3	3	-	-	1	1	-	-	2	-
CO4	3	2	3	2	3	-	-	2	2	-	1	3	2

Course Title	FPGA System Design Lab		
Course Code	25VL406	**(L-T-P) C**	(0-0-2)1
Exam	3	**Hours/Week**	2
SEE	50 marks	**Total Hours**	28P+2E=30

Course objectives: To provide students with practical knowledge of FPGA-based digital system design using Hardware Description Languages (HDLs) and FPGA development tools. The course enables students to design, implement, interface, test, and optimize FPGA-based embedded systems by integrating peripherals, sensors, communication modules, and real-time hardware applications to solve application-oriented open-ended engineering problems.

Course Outcomes (COs):
Upon completion of the course, students shall be able to:

COs	Statement	POs	PSOs
1.	Design, implement, and verify digital systems on an FPGA platform using Hardware Description Languages (HDLs) and FPGA development tools.	1, 2, 3, 4, 5, 8, 9, 11	1,2
2.	Interface FPGA with peripheral devices, sensors, communication modules, displays, and motor control circuits to develop embedded hardware applications.	1, 2, 3, 4, 5, 8, 9, 11	1,2
3.	Design, implement, test, and evaluate FPGA-based embedded systems by integrating hardware peripherals and communication interfaces to solve application-oriented and open-ended engineering problems.	1, 2, 3, 4, 5, 8, 9, 11	1,2

ABL: Lab based learning (28Hrs.)

Sl. No.	PART-A: Fixed Experiments
1	Interface 16 switches with 16 SMD LEDs and verify digital input-output operations.
2	Interface 4 push buttons with 2 RGB LEDs and implement control logic.
3	Interface and control a 4-digit seven-segment display**.**
4	Interface a buzzer and generate tones using PWM.
5	Interface a DC motor and implement PWM-based speed control.
6	Interface a stepper motor and control its direction and rotation sequence.
7	Interface an LCD and keyboard for user interaction.
8	Interface an Analog-to-Digital Converter (ADC) and acquire analog sensor data.

9	Interface a Digital-to-Analog Converter (DAC) and generate analog output signals.
10	Interface a relay module for switching applications.
Sl. No.	**PART-B: Open-ended Experiments**
1	Develop an FPGA-based **digital door lock** using keypad and password authentication.
2	Design an FPGA-based **smart home automation system** using relay and sensor interfaces.
3	Develop an FPGA-based **environmental monitoring system** using temperature, gas, and ultrasonic sensors.
4	Develop an FPGA-based **digital clock with alarm** using a seven-segment display and push buttons.
5	Design an FPGA-based **motor control system** integrating DC motor, stepper motor, and PWM techniques.
6	Design an FPGA-based **IoT-enabled sensor monitoring system** integrating multiple sensors and wireless communication.

Proposed Assessment Plan for 50 marks:

Tool	Remarks	Marks
Assessment method	Continuous Evaluation Record Writing Lab CIE	10 20 20
Total		**50**

Teaching-Learning–Evaluation Scheme:

Sl. No	Teaching and Learning Method	No. of Hours/Week	No. of Weeks	Hours/ Semester
1	Lab Conduction	2	14	28
2	Evaluation	-	-	02
Total Learning Hours/Semester				30

Reference Books:

1. **Pong P. Chu**, *FPGA Prototyping by Verilog Examples: Xilinx Spartan-3 Version*, Wiley India, 2008.
2. **Samir Palnitkar**, *Verilog HDL: A Guide to Digital Design and Synthesis*, 2nd Edition, Pearson Education, 2003.
3. **Wayne Wolf**, *FPGA-Based System Design*, Prentice Hall, 2004.

Online Courses and Video Lectures:

1. https://www.amd.com/en/products/adaptive-socs-and-fpgas.html
2. https://www.amd.com/en/corporate/university-program/adaptive-computing-training.html
3. https://learningcatalog-amd.netexam.com/Certification/58546/designing-fpgas-using-the-vivado-design-suite-1

Course Articulation Matrix:

Course Outcomes	**Program Outcomes**												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**
CO1	3	2	3	2	3	-	-	2	1	-	1	3	3
CO2	2	2	3	2	3	-	-	2	2	-	1	3	3
CO3	2	3	3	3	3	-	-	2	2	-	1	3	3

Course Title	SPICE Programming for Electronic Circuits		
Course Code	25VL407A	**(L-T-P) C**	(0-0-2)1
Exam	3	**Hours/Week**	2
SEE	50 marks	**Total Hours**	28P+2E=30

Course Objective: To provide students with practical knowledge of electronic circuit simulation using LTspice/Ngspice and SPICE netlist development. The course enables students to design, simulate, analyze, validate, and optimize analog and MOSFET-based electronic circuits through DC, AC, and transient analyses while solving application-oriented open-ended circuit design problems.

Course Outcomes (COs) {with mapping shown against the Program Outcomes (POs)}
Upon completion of the course, students shall be able to:

COs	Statement	POs	PSOs
1.	Develop SPICE netlists and perform DC, AC, and transient simulations of electronic circuits using LTspice/Ngspice.	1, 2, 3, 4, 5, 8, 9, 11	1
2.	Analyze and evaluate the characteristics of passive networks, rectifier circuits, filters, and MOSFET-based circuits through simulation and waveform interpretation.	1, 2, 3, 4, 5, 8, 9, 11	1
3.	Design, simulate, validate, and optimize application-oriented electronic circuits using SPICE tools to solve open-ended engineering problems involving analog and CMOS circuits.	1, 2, 3, 4, 5, 8, 9, 11	1

Teaching-Learning–Evaluation Scheme:

Sl. No	Teaching and Learning Method	No. of Hours/Week	No. of Weeks	Hours/ Semester
1	Lab Conduction	2	14	28
2	Evaluation	-	-	02
Total Learning Hours/Semester				30

ABL: Lab based learning (28Hrs.)

Sl. No.	PART-A: Fixed Experiments
1	Familiarization with the LTspice/Ngspice environment and basic SPICE commands.
2	Develop a SPICE netlist for a resistive network and verify Ohm's Law using DC sweep analysis.
3	Develop SPICE netlists and analyze the transient response of RC low-pass and high-pass circuits.
4	Develop SPICE netlists and analyze the transient and AC response of RL low-pass and high-pass circuits.

5	Develop SPICE netlists and perform AC analysis of RC low-pass and high-pass filters with and without parasitic inductance.
6	Develop SPICE netlists and simulate diode rectifier and clipping circuits.
7	Develop a SPICE netlist and perform AC analysis of an RLC circuit and obtain its frequency response.
8	Develop a SPICE netlist and study the frequency response and Bode plot of a circuit.
9	Develop SPICE netlists and simulate MOSFET drain characteristics (ID–VDS) and transfer characteristics (ID–VGS).
10	Develop SPICE netlists and simulate a common-source MOSFET amplifier, MOSFET inverter, CMOS inverter, and buffer circuit using inverter subcircuits.
Sl. No.	**PART-B: Open-ended Experiments**
1	Design and simulate a regulated DC power supply using rectifier, filter, and voltage regulation circuits.
2	Design and optimize an RC or RL filter for a specified cutoff frequency and performance requirement.
3	Develop a SPICE model to compare the performance of different rectifier configurations under varying load conditions.
4	Design and simulate a MOSFET-based switching circuit for power or digital applications.
5	Develop a multi-stage MOSFET amplifier to achieve a specified voltage gain and bandwidth.
6	Design and simulate a CMOS logic circuit such as NAND, NOR, XOR, or a simple combinational block using SPICE netlists.

Proposed Assessment Plan for 50 marks:

Tool	Remarks	Marks
Assessment method	Continuous Evaluation Record writing Lab CIE	10 20 20
Total		**50**

Textbooks:

1. SPICE for Circuits and Electronics Using PSpice, M. H. Rashid, SPICE for Circuits and Electronics Using PSpice. Upper Saddle River, NJ, USA: Pearson Education, 2004.
2. The SPICE Book, A. Vladimirescu, The SPICE Book. New York, NY, USA: John Wiley & Sons, 1994.

Reference books / Manuals:

1. Purdue University, SPICE user manual: https://www.physics.purdue.edu/~jones105/phys536_Spring2008/Spice3F4_Manual.pdf
2. HSPICE® User Guide: Simulation and Analysis - https://cseweb.ucsd.edu/classes/wi10/cse241a/assign/hspice_sa.pdf

Web links and Video Lectures (e-Resources):

- IITR lecture – "Introduction to spice":
  - https://www.youtube.com/watch?v=KfBtduxuxCw
- IITR lecture – "SPICE Simulation":
  - https://www.youtube.com/watch?v=Z6Cfbs0ODpg
  - https://www.youtube.com/watch?v=tI5GLv1ipKw

Recommended Tools:

Free circuit simulation tools such as **LTspice and Ngspice**, or commercial VLSI ECAD software packages such as Siemens, Cadence, Altium etc.

Course Articulation Matrix

Course Outcomes	Program Outcomes												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**
CO1	3	2	2	2	3	-	-	2	1	-	1	3	-
CO2	3	3	2	3	3	-	-	2	1	-	1	3	-
CO3	3	3	3	3	3	-	-	2	2	-	1	3	-

Course Title	Power Electronics		
Course Code	25VL407B	(L-T-P) C	(0-0-2)1
Exam	3	Hours/Week	2
SEE	50 marks	Total Hours	28P+2E=30

Course Objective: To provide students with practical knowledge of power semiconductor devices and power electronic converters through laboratory experiments. The course enables students to design, analyze, implement, test, and evaluate power electronic circuits using modern measurement techniques while solving application-oriented open-ended problems involving power conversion and control systems.

Course Outcomes (COs) with mapping shown against the Program Outcomes (POs)
Upon completion of the course, students shall be able to:

COs	Statement	POs	PSOs
1.	**Identify, characterize, and analyze** the operating characteristics of power semiconductor devices used in power electronic circuits.	1, 2, 4, 5, 8, 9, 11	1
2.	**Design, implement, and evaluate** rectifiers, DC–DC converters, inverters, and PWM-based power electronic circuits using appropriate testing and measurement techniques.	1, 2, 3, 4, 5, 8, 9, 11	1
3.	**Design, test, and optimize** application-oriented power electronic systems by integrating power semiconductor devices and converters to solve open-ended engineering problems.	1, 2, 3, 4, 5, 8, 9, 11	1

Teaching-Learning–Evaluation Scheme:

Sl. No	Teaching and Learning Method	No. of Hours/Week	No. of Weeks	Hours/ Semester
1	Lab Conduction	2	13	26
2	Evaluation	-	-	02
Total Learning Hours/Semester				28

ABL: Lab based learning (28Hrs.)

Sl. No.	PART-A: Fixed Experiments
1	Study and identify power semiconductor devices used in power electronic systems.
2	Obtain the V–I characteristics of a power diode.
3	Obtain the V–I characteristics of an SCR.
4	Implement and analyze a half-wave rectifier with a resistive load.
5	Implement and analyze a full-wave rectifier with a resistive load.

6	Implement and analyze a controlled rectifier using an SCR.
7	Study and demonstrate the operation of a DC chopper circuit.
8	Implement and analyze a step-down (Buck) DC–DC converter.
9	Implement and analyze a step-up (Boost) DC–DC converter.
10	Implement and analyze a single-phase inverter and study PWM control and output waveforms.
Sl. No.	**PART-B: Open-ended Experiments**
1	Design and implement a regulated DC power supply using rectifiers, filter, and voltage regulator circuits.
2	Design and evaluate a variable DC motor speed control system using PWM techniques.
3	Design and implement a battery charging circuit using a DC–DC converter.
4	Develop a power converter with adjustable output voltage for a specified load.
5	Design and implement an LED driver circuit using a switching converter.
6	Develop a PWM-based inverter for variable-frequency AC output.

Proposed Assessment Plan for 50 marks:

Tool	Remarks	Marks
Assessment method	Continuous Evaluation Record writing Lab CIE	10 20 20
Total		**50**

Textbooks:

1. Power Electronics: Circuits, Devices and Applications, M. H. Rashid, Power Electronics: Circuits, Devices and Applications, 4th ed. Noida, India: Pearson Education, 2014.
2. Power Electronics, P. S. Bimbhra, Power Electronics, 5th ed. New Delhi, India: Khanna Publishers, 2012.

Web links and Video Lectures (e-Resources):

1. https://www.youtube.com/watch?v=jydMBLSh7iI&list=PLSnw1KE0TFkVu05Ws0Ax143gZYmxPMCoY

Course Articulation Matrix

Course Outcomes	Program Outcomes												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**
CO1	3	2	-	1	2	-	-	2	1	-	1	2	-
CO2	3	3	2	3	3	-	-	2	2	-	1	2	-
CO3	2	3	2	3	3	-	-	2	2	-	1	2	-

Course Title	Data structures using python		
Course Code	25VL407C	(L-T-P) C	(0-0-2)1
Exam	3	Hours/Week	2
SEE	50 marks	Total Hours	28P+2E=30

Course Objective: To provide students with practical knowledge of implementing data structures and algorithms using Python. The course enables students to design, implement, analyze, and optimize data structures and algorithms to solve application-oriented computational problems through programming and open-ended problem-solving approaches.

Course Outcomes (COs) {with mapping shown against the Program Outcomes (POs)}
Upon completion of the course, students shall be able to:

COs	Statement	POs	PSOs
1.	Design and implement fundamental linear data structures such as arrays, stacks, queues, and linked lists using Python.	1, 2, 3, 4, 5, 8, 9, 11	1
2.	Apply appropriate data structures and algorithms for searching, sorting, and solving computational problems using Python.	1, 2, 3, 4, 5, 8, 9, 11	1
3.	Design, implement, test, and evaluate application-oriented Python programs by integrating suitable data structures and algorithms to solve open-ended engineering problems.	1, 2, 3, 4, 5, 8, 9, 11	1

Teaching-Learning–Evaluation Scheme:

Sl. No	Teaching and Learning Method	No. of Hours/Week	No. of Weeks	Hours/ Semester
1	Lab Conduction	2	14	28
2	Evaluation	-	-	02
Total Learning Hours/Semester				30

ABL: Lab based learning (28Hrs.)

Sl. No.	PART-A: Fixed Experiments
1	Implement array traversal and basic array operations.
2	Implement insertion and deletion operations in an array.
3	Implement Linear Search and Binary Search algorithms.
4	Implement Stack operations using arrays.

5	Develop a program to check balanced parentheses using a stack.
6	Implement Infix-to-Postfix expression conversion using a stack.
7	Implement Queue operations using arrays.
8	Implement Circular Queue operations.
9	Implement creation and traversal of a singly linked list.
10	Implement insertion, deletion, reversal, and sorting algorithms (Bubble Sort and Selection Sort) using Python.
Sl. No.	**PART-B: Open-ended Experiments**
1	Design and implement a student record management system using appropriate data structures.
2	Develop a menu-driven application for library management using linked lists and queues.
3	Design a browser history management system using stacks.
4	Develop a railway or bus reservation queue management system.
5	Design a polynomial manipulation program using linked lists.
6	Develop an expression evaluator using stacks and queues.

Proposed Assessment Plan for 50 marks:

Tool	Remarks	Marks
Assessment method	Continuous Evaluation Record writing Lab CIE	10 20 20
Total		**50**

Textbook:

Sl. No	Book Title	Authors	Edition	Publisher	Year
1	Data Structures and Algorithms Using Python	R. D. Necaise	1st	Hoboken, NJ, USA: Wiley	2016
2	Data Structures and Algorithms Made Easy	N. Karumanchi	1st	Career Monk Publications	2018

Web links and Video Lectures (e-Resources):

1. https://www.youtube.com/watch?v=_uQrJ0TkZlc
2. https://www.youtube.com/watch?v=nLRL_NcnK-4
3. https://www.youtube.com/playlist?list=PLdo5W4Nhv31bbKJzrsKfMpo_grxuLl8LU

Course Articulation Matrix

Course Outcomes	Program Outcomes												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**
CO1	2	3	2	1	3	-	-	2	1	-	1	2	2
CO2	2	3	3	2	3	-	-	2	1	-	1	2	2
CO3	2	3	3	2	3	-	-	2	2	-	1	2	3

Course Title	Python for Measurement & Data Analysis		
Course Code	25VL407D	(L-T-P) C	(0-0-2)1
Exam	3	Hours/Week	2
SEE	50 marks	Total Hours	28P+2E=30

Course Objective: To provide students with practical knowledge of Python programming for scientific and engineering applications involving numerical computation, measurement data analysis, and visualization. The course enables students to develop, analyze, visualize, and interpret experimental data using Python libraries such as NumPy, Pandas, and Matplotlib while solving application-oriented open-ended engineering problems.

Course Outcomes (COs) {with mapping shown against the Program Outcomes (POs)}
Upon completion of the course, students shall be able to:

COs	Statement	POs	PSOs
1.	Develop Python programs using NumPy to perform numerical computation and scientific data processing.	1, 2, 3, 4, 5, 8, 9, 11	1
2.	Analyze, manipulate, and visualize engineering measurement data using Pandas, Matplotlib, and appropriate statistical techniques.	1, 2, 3, 4, 5, 8, 9, 11	1
3.	Design, implement, test, and evaluate Python-based solutions for application-oriented measurement, data analysis, and visualization problems using appropriate scientific computing libraries.	1, 2, 3, 4, 5, 8, 9, 11	1

Teaching-Learning–Evaluation Scheme:

Sl. No	Teaching and Learning Method	No. of Hours/Week	No. of Weeks	Hours/ Semester
1	Lab Conduction	2	14	28
2	Evaluation	-	-	02
Total Learning Hours/Semester				30

ABL: Lab based learning (28Hrs.)

Sl. No.	PART-A: Fixed Experiments
1	Introduction to the Python programming environment and basic programming constructs.
2	Perform numerical computations using Python.
3	Implement array operations using the NumPy library.
4	Perform matrix operations using NumPy.
5	Read experimental measurement data from CSV files.

6	Perform data manipulation and preprocessing using Pandas.
7	Plot engineering and experimental data using Matplotlib.
8	Plot and compare multiple signals using different graph formats.
9	Generate scatter plots for sensor measurement data analysis.
10	Perform statistical analysis, histogram generation, correlation analysis, and simple signal analysis using Python.
Sl. No.	**PART-B: Open-ended Experiments**
1	Design and develop a Python application to analyze temperature sensor data and generate graphical reports.
2	Develop a Python-based data acquisition and visualization program for engineering measurements stored in CSV files.
3	Design a Python application to compare the performance of multiple experimental datasets using statistical analysis.
4	Develop an automated measurement data processing system with data cleaning, filtering, and visualization.
5	Design a Python application for real-time monitoring and visualization of simulated sensor data.
6	Develop a fault detection system by analyzing measurement data using statistical techniques.

Proposed Assessment Plan for 50 marks:

Tool	Remarks	Marks
Assessment method	Continuous Evaluation Record writing Lab CIE	10 20 20
Total		**50**

Textbooks:

1. W. McKinney, Python for Data Analysis. Sebastopol, CA, USA: O'Reilly Media 2012. Q. Kong, T. Siauw, and A. Bayen, Python Programming and Numerical Methods: A Guide for Engineers and Scientists. Cambridge, MA, USA: Academic Press, 2020.

Web links and Video Lectures (e-Resources):

1. Complete Python for Data Science Course https://glasp.co/youtube/p/python-for-data-science-course-for-beginners-learn-python-pandas-numpy-matplotlib
2. Data Analysis with Python Full Course https://www.youtube.com/watch?v=r-uOLxNrNk8
3. NumPy Full Tutorial https://www.datakwery.com/freecodecamp/numpy/

Course Articulation Matrix

Course Outcomes	Program Outcomes												
COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**
CO1	2	3	2	1	3	-	-	2	1	-	1	2	-
CO2	2	3	2	3	3	-	-	2	2	-	1	2	-
CO3	2	3	3	2	3	-	-	2	2	-	1	2	-

Semester:IV						
PHYSICAL EDUCATION (SPORTS & ATHLETICS)– II						
Course Code	**:**	25PE2		**CIE**	**:**	**100 Marks**
Course Type	**:**	NCMC				
Total Hours	**:**	15 P				

Course Outcomes: At the end of the course, the student will be able to

1. Understand the ethics and moral values in sports and athletics
2. Perform in the selected sports or athletics of student's choice.
3. Understand the roles and responsibilities of organization and administration of sports and games.

Module I: Ethics and Moral Values **4 Hours**

A. Ethics in Sports
B. Moral Values in Sports and Games

Module II : Specific Games (Any one to be selected by the student) **16 Hours**

A. Volleyball –Attack, Block, Service, Upper Hand Pass and Lowerhand Pass.
B. Athletics (Track Events) –Any event as per availability of Ground.

Module III : Role of organisation and administration **4 Hours**

Scheme and Assessment for auditing the course and Grades:

Sl.No.	Activity	Marks
1.	Participation of student in all the modules	20
2.	Quizzes/Assignment–2,eachof 20marks	40
3.	Final presentation/exhibition/Participation in competitions/ practical on specific tasks assigned to the students	40
	Total	**100**

Semester IV			
Yoga - II			
Course Code	25YOG2	**CIE**	100 Marks
Course Type	NCMC		
Total Hours	2 hrs/week		

Course Objectives

The objectives of this course are to:

1. Introduce students to the origin, history, philosophy, and fundamental concepts of Yoga.
2. Familiarize students with the different schools of Yoga, its aims, objectives, and the importance of prayer in Yogic practice.
3. Develop awareness of the rules, regulations, and safety precautions to be followed during Yogic practices.
4. Enable students to learn and practice Suryanamaskara and selected Yogasanas with proper techniques for improving physical and mental well-being.
5. Promote a healthy life style by encouraging regular Yogic practice, correcting misconceptions about Yoga, and fostering positive health, self-discipline, and overall wellness.

Patanjali's Ashtanga Yoga: Patanjali's Ashtanga Yoga, its need and importance. Yama: Ahimsa, satya, asteya, brahmacharya, aparigraha, Niyama : shoucha, santosh, tapa, svaadhyaya, Eshvarapranidhan, Suryanamaskar 12 count 4 rounds. Different types of Asanas: Sitting 1. Sukhasana, 2.Paschimottanasana, Standing1. Ardhakati Chakrasana, 2.ParshvaChakrasana, Prone line 1. Dhanurasana Supine line 1. Halasana, 2. Karna Peedasana

Kapalabhati: Meaning, importance and benefits of Kapalabhati. 40strokes/min3 rounds Pranayama–1. Suryanuloma–Viloma, 2.Chandranuloma-Viloma, 3-Suryabhedana, 4-Chandra Bhedana, 2.Nadishodhana, 3-BhramariPranayama, Meaning, Need, importance of Pranayama. Different types. Meaning by name, technique, precautionary measures and benefits of each Pranayama

Course Outcomes:

Upon successful completion of this course, the student will be able to:

1. Explain the origin, history, philosophy, objectives, and different schools of Yoga, along with its role in promoting holistic health and well-being.
2. Understand and apply the rules, regulations, and ethical practices associated with Yogic exercises, including the significance of prayer and Suryanamaskara.
3. Demonstrate the correct techniques of selected Yogasanas, such as sitting, standing, prone, and supine postures, while observing appropriate precautions.
4. Analyze the physical, mental, and therapeutic benefits of Yogic practices and distinguish between authentic Yogic practices and common misconceptions about Yoga.
5. Adopt Yoga as a regular life style practice to enhance physical fitness, mental wellness, discipline, and overall quality of life.

Suggested Learning Resources: (TextBook/ReferenceBook/Manuals):

Text books:

1. George Feuerstein: the yoga Tradition (its history, literature, philosophy and practice)
2. Sri Ananda: The complete Book of yoga Harmony of Body and Mind (Orient paper Backs: Vision Books Pvt.Ltd..1982.
3. B.K.Slyenkar: Light on the Yoga sutras of Patanjali (Haper Collins Publications India Pvt.Ltd.New Delhi.)
4. Science of Divinity and Realization of Self Vethathiri Publication,(6-11)WCSC,Erode

Reference books/Manuals:

1. Principles and Practice of Yoga in Health Care,Publisher:Handspring Publishing Limited. ISBN:9781909141209,978190914209
2. BasavaraddiIV: Yoga in School Health, MDNIY NewDelhi. 2009
3. Dr.HR.Nagendra: Yoga Research and application (Vivekanda Kendra Yoga Prakashana Bengalore)
4. Dr.Shirley Telles: Glimpses of Human Body (Vivekanda KendraYoga Prakashana Bengalore).

Web links and Video Lectures (e-Resources):

Search by topics to get the videos

Assessment Structure:

This course is having only **Continuous Internal Assessment** (CIE) marks of 100.

Weightage	**Marks**
Attendance to all the sessions	20Marks
Practical sessions on Yoga and Its Benefits	40Marks
Two Assignments	40Marks
Total Marks	100

A student shall obtain a minimum of 40% marks or 40 marks out of 100 to qualify in the course.