Field Effect Transistors

3.1 Introduction:

- The Field Effect Transistor abbreviated as FET is an another semiconductor device like a BJT which can be used as an amplifier or switch. Like BJT, FET is also a three terminal device. However, the principle of operation FET is completely different from that of BJT.
- The three terminals of FET's are named as: **Drain (D), Source (S) and Gate (G),** as shown in Fig. 2. Out of these terminals gate terminal acts as a controlling terminal.

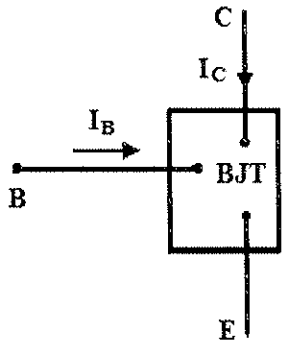


Fig.1

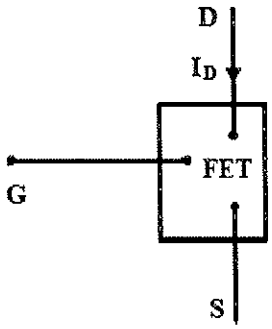
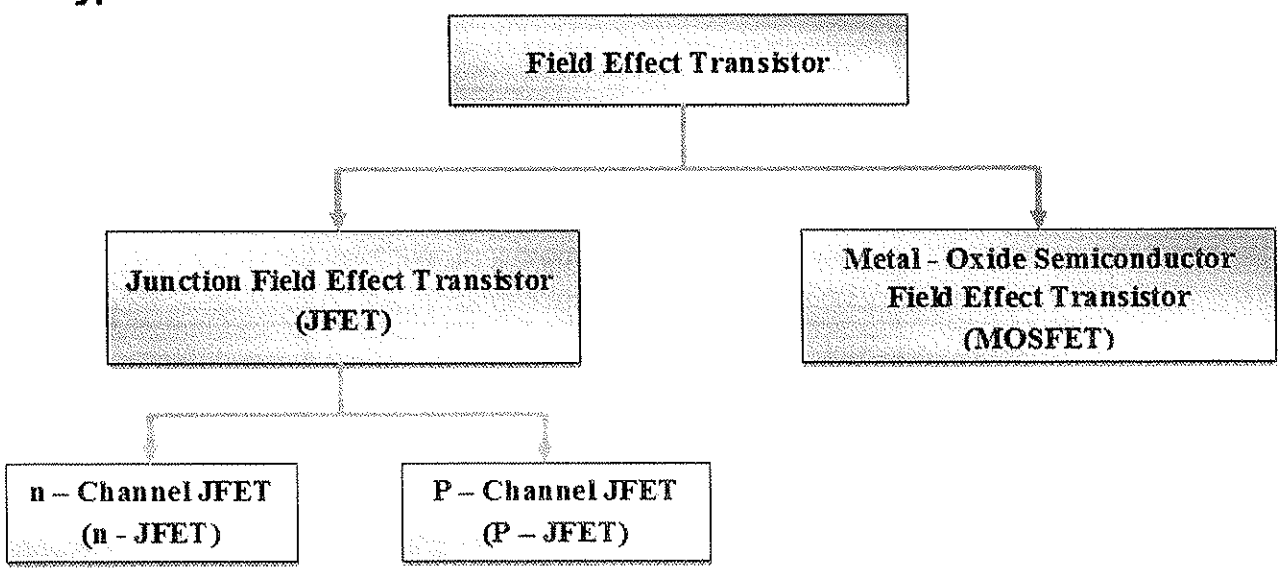


Fig. 2

- In BJT the output current, I_C is controlled by the base current I_B. Hence BJT is a current controlled device. On the other hand, in FET, the voltage applied between gate and source (V_{GS}) controls the output current I_D therefore; **FET is a voltage controlled device.**
- The name "**Field Effect**" is derived from the fact that the output current flow is controlled by an electric field set up in the device by an externally applied voltage between gate and source terminals (V_{GS}).
- BJT is called a bipolar device because here, the conduction of current is due to both electrons and holes (both Majority & Minority charge carriers). However, FET is called a **unipolar device** because here, the conduction of current is only due to majority charge carriers. (electrons in n-JFET and holes in p - JFET).

3.2 Types of FET:



3.3 Schematic symbol of JFET:

Figure 3 & 4 shows the schematic symbol of JFET. In an n-channel JFET, the arrow points towards the vertical line (shown in Fig. 3) and in p-channel JFET, the arrow points away from the vertical line (shown in Fig. 4). The vertical line represents the channel.

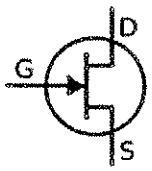


Fig. 3 *n-channel JFET*

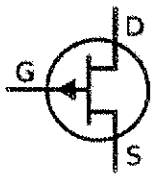
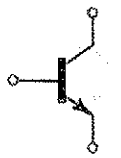
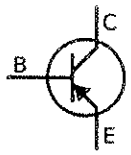
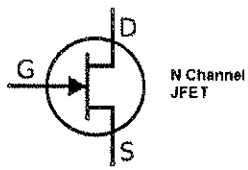
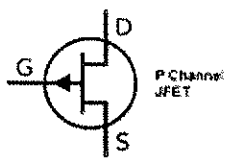


Fig. 4 *p-channel JFET*

3.4 Comparison of BJT & FET:

	BJT	FET
1)	BJT is a current controlled device.	JFET is a voltage controlled device.
2)	Two types of transistors are npn & pnp type.	Two types of transistors are n-JFET & p-JFET.
3)	 npn  pnp	 
4)	BJT is a **Bipolar device.**	FET is an **Unipolar device.**
5)	Input impedance is low.	Input impedance is high.
6)	BJTs are less temperature stable.	FETs are more temperature stable.
7)	Bigger in size.	Smaller in size, hence suitable for IC chips.
8)	More sensitivity to changes in the applied signal.	Less sensitivity to changes in the applied signal.
9)	Thermal runaway may occur.	Thermal runaway does not occur.
10)	Input and output relation is linear.	Input and output relation is non linear.

JFET	BJT
source S	emitter E
drain D	collector C
gate G	base B
drain supply V_{DD}	collector supply V_{CC}
gate supply V_{GG}	base supply V_{BB}
drain current i_D	collector current i_C

3.5 Reasons for popularity:

- Operation of FET is very simple (as compared to BJT).
- Design or fabrication is much simpler. It can be fabricated in fewer steps.
- Occupy small space (the area required for a single FET on chip is $1/5^{th}$ of BJT).
- It consumes low power (in micro watts).

NOTE: *The thickness of the depletion region increases as the reverse bias voltage across the junction is increased. The extension of the depletion region depends on the doping levels of p-type & n-type semiconductors. If both the regions are equally doped, the depletion region will extend equally on both the regions. However, if one of the regions is heavily doped in comparison with the other region, the depletion region extends more into the region of lower doping.*

3.6 Construction and characteristics of n- channel JFET:

- The basic construction of the n-channel JFET is shown in Fig. 5. The major part of the structure is the *n*-type material that forms the channel between the embedded layers of *p*-type material. *(here p-type materials are heavily doped)*
- The top of the *n*-type channel is connected through an ohmic contact to a terminal referred to as the **drain (D)**, while the lower end of the same material is connected through an ohmic contact to a terminal referred to as the **source (S),** both the p-type regions are connected internally and a single wire is taken out in the form of a terminal called the **gate (G).**

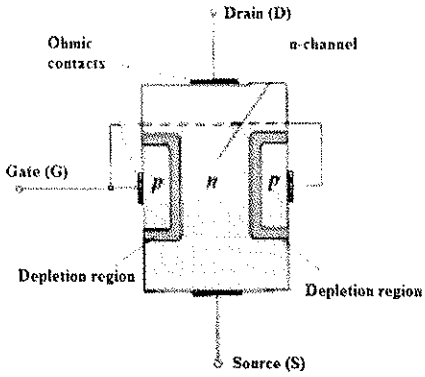


Fig. 5

- In the absence of any applied potentials (under no-bias conditions) the JFET has two *p-n* junctions. The result is a depletion region at each junction as shown in Fig. 5. Depletion does not allow majority carriers to flow through the region, but field created can control the majority carriers through the channel.

The following FET notation is worth remembering:

- **Source**: The Source S is the terminal through which majority carriers enter the channel (n region). Conventional current leaving the channel is designated by **Is**. Since majority carriers come from it, it is called source.
- **Drain**: The drain D is the terminal through which the majority carriers leave the region that is they are drained out from this terminal. Conventional current entering the region at D is designated by I_D. The drain to source voltage is called V_{DS}.
- **Gate**: On both the sides of the n-type region of Fig.5, heavily doped regions of p (that is p^+) are grown that creates p-n junctions. These two p-type materials are connected together (internally shorted) and a single wire is taken out in the form of a terminal called a gate. Between the gate & source a voltage V_{GS} is applied. (Here, both the gate terminals are connected together that means when we apply a voltage, the voltage will apply simultaneously on both the gates)
- **Channel:** It is the space or region between the two gate regions (two p regions) through which majority carriers move from source to drain when V_{DS} is applied.

NOTE: *The construction of p-channel JFET is similar to that of n-channel JFET, consisting of p type channel and n type gate.*

3.6.1 Operation (Working) of n-channel JFET:

Let us now consider an ***n-channel*** *JFET and discuss its working:*

(1) When $V_{GS} = 0$ and $V_{DS} = 0$

In this case, drain current $I_D = 0$, because $V_{DS} = 0$. The depletion regions around the *p-n* junctions are of equal thickness and symmetrical as shown in Fig. 5.

(2) When $V_{GS} = 0$ and V_{DS} is increased from zero (V_{DS} some positive value)

- In Fig. 6, a positive voltage V_{DS} has been applied across the channel and the gate has been connected directly to the source to establish the condition $V_{GS} = 0$ V.
- The result is a gate and source terminal at the same potential and a depletion region in the low end of each *p*-material (near to the source region) similar to the distribution of the no-bias conditions of Fig. 5.
- The voltage V_{DS} is applied across drain to source. The drain is made positive with respect to source.
- The instant the voltage V_{DS} is applied, The electrons (which are the majority carriers) flow from *S* to *D* whereas *conventional drain current I_D flows through the channel from D to S.*

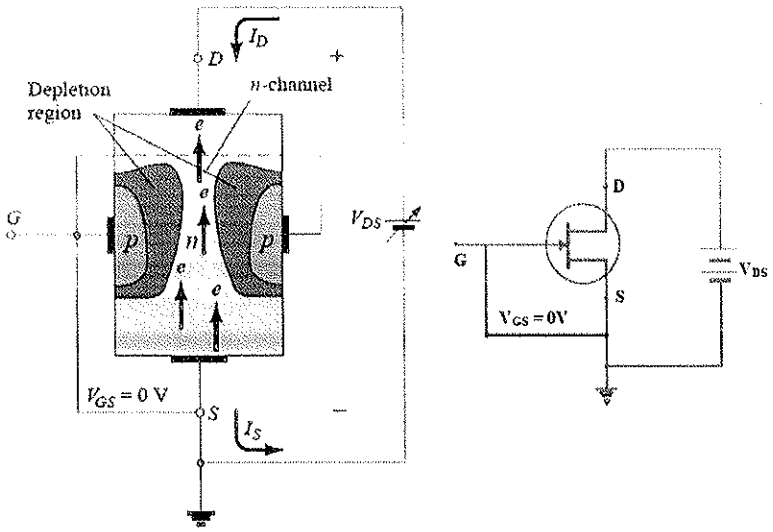


Fig. 6 *JFET at $V_{GS} = 0V$ and $V_{DS} > 0V$*

- Since the p region of an n–channel JFET is heavily doped, as compared to the n–channel, the depletion region extends less into the p region and deeper into the n–channel as shown in Fig. 6.
- It is important to note that the depletion region penetrates more deeply into the n-channel near the drain terminal and less near the source terminal.
- This is because the channel has some finite resistance, it will cause some voltage drop across the channel. The voltage drop nearer to the drain terminal is more compared to source terminal, due to this reverse bias voltage is higher near the drain end of the channel as compared to the source end. So the depletion region extends more deeply into the n-channel near the drain terminal.

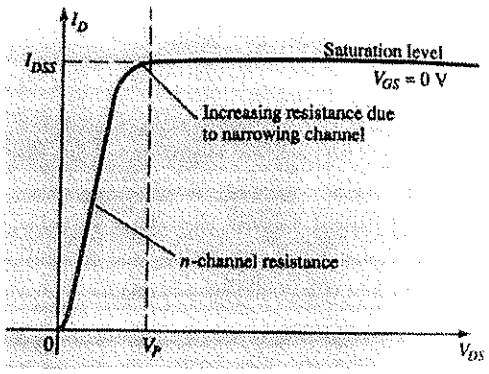


Fig. 7 I_D versus V_{DS} for V_{GS}=0V

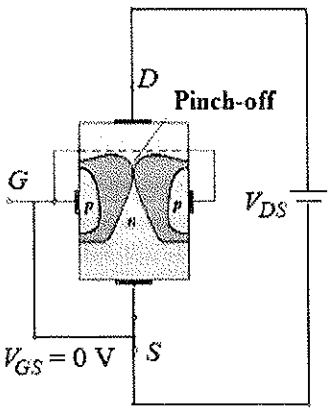


Fig. 8

- As the voltage V_{DS} is increased from zero, the current I_D in channel increases according to ohm's law as shown in Fig. 7.
- As V_{DS} increases, the depletion regions widens, causing a noticable reduction in the channel width. The reduced path of conduction causes the resistance to increase and the drain current I_D reaches saturation because of this.
- If V_{DS} is increased to a level where two depletion regions will "*touch*" each other as shown in Fig. 8, is known as ***pinch-off***. The level of V_{DS} that establishes this condition is referred to as the ***pinch-off voltage*** and is denoted by V_P as shown in Fig. 7.

- After pinch-off voltage, the channel width becomes so narrow (very less) that depletion layers almost touch each other (shown in Fig. 9). The drain current passes through the small passage between these layers. Therefore I_D remains constant, when V_{DS} is increased beyond V_P.
- The current flow from drain to source when $V_{DS} > V_P$ & $V_{GS} = 0V$ is known as drain to source current with a short circuit from gate to source & it is denoted by I_{DSS}.
- I_{DSS} is the maximum drain current for a JFET & is defined by conditions $V_{DS} > V_P$ & $V_{GS} = 0V$.
- I_{DSS} = Drain to Source current when the gate & source terminals are short circuited.

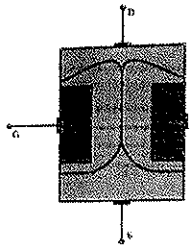


Fig. 9

(3) When $V_{GS} < 0V$ (that means negative voltage, V_{GS} = -ve) and $V_{DS} > 0$

- Negative voltage is applied between gate and source of FET as shown in Fig. 10.
- The effect of the applied negative bias is to establish depletion regions similar to those obtained with $V_{GS} = 0V$, but at lower levels of V_{DS}.
- Therefore, the result of applying a negative bias to the gate is to reach saturation level at a lower level of V_{DS} as shown in Fig. 11.

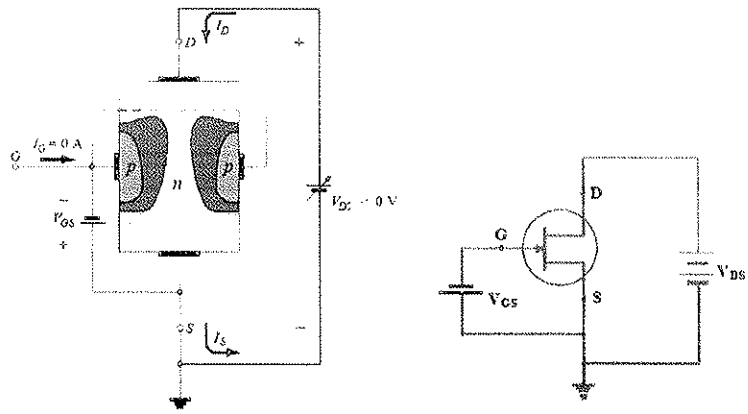


Fig. 10 *Application of a negative voltage to the gate of a JFET*

- The resulting saturation level for I_D has been reduced and in fact will continue to decrease as V_{GS} is made more & more negative. *(as shown in Fig. 11)*

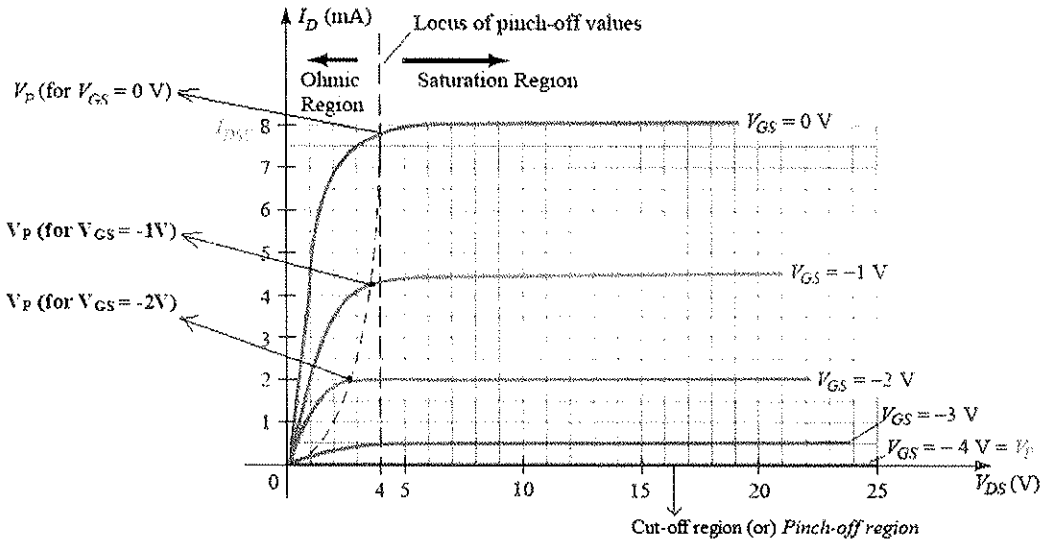


Fig. 11 *n-channel JFET characteristics with I_{DSS} = 8mA & V_P = -4V*

- When V_{GS} is sufficiently negative where drain current I_D = 0 mA, the device is ***"turned-off"***. At this point V_{GS} = - V_P. *(device is in cut-off region)*
- The level of V_{GS} that results in I_D = 0 mA is defined as V_{GS} = - V_P for n-channel (V_{GS} = + V_P for p-channel JFET).

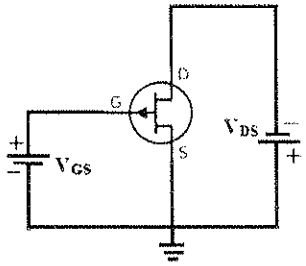


Fig. 12

NOTE: *The working of p-channel JFET is exactly similar to that of n-channel JFET except that the* ***current carriers are holes*** *and polarities of both the voltage sources* V_{GS} & V_{DS} *are reversed. It means that* V_{GS} *would be positive for a p-channel* JFET *and* V_{DS} *is negative as shown in Fig. 12. Here, Drain terminal is connected to negative and Source is connected to positive terminal of the battery.*

3.7 Output characteristics (Drain characteristics) of n- channel JFET:

The graph of drain current (I_D) *versus drain-to-source voltage* (V_{DS}) *at constant gate-to-source voltage* (V_{GS}) *is termed as* ***drain characteristics or output characteristics.***

Drain characteristics of n-channel JFET is shown in Fig. 11 and has been already discussed in the section 3.6.1. It can be subdivided into three regions:

1) **Ohmic region:** (For $V_{DS} > 0$ and $V_{DS} < V_P$)
The region to the left of the pinch-off locus of Fig. 11 is referred to as the ohmic region. For lower values of V_{DS} depletion layer of the channel is very small and the JFET acts like a voltage controlled resistor and the curve is almost linear. That means as the voltage V_{DS} is incresed from zero, the current I_D also increases proportionally according to ohms law ($\mathbf{I \propto V}$). So this region is called ohmic region.

2) **Saturation region :**
After pinch-off voltage, the channel width becomes so narrow (very small) that depletion layers almost touch each other. The drain current I_D passes through the small passage between these layers. Therefore, increase in drain current is very small with V_{DS} above pinch-off voltage. Consequently drain current remains constant.

From Fig. 13, It is seen that with $V_{GS} = 0$, I_D saturates at I_{DSS} and the characteristic shows $V_{DS} = 4V$. When an external bias of $V_{GS} = -1$ V is applied, I_D saturates at $V_{DS} = 3V$. (The effect of the applied negative bias is to establish depletion regions similar to those obtained with $V_{GS} = 0V$, but at lower levels of V_{DS}) Similarly when $V_{GS} = -2V$, I_D saturates at $V_{DS} = 2V$ and so on.

Therefore, the result of applying a negative bias to the gate is to reach saturation level at a lower level of V_{DS} as shown in Fig. 11 & Fig. 13.

Since, I_D *remains constant (saturates) irrespective of the rise in voltage* V_{DS} *this region is called saturation region.*

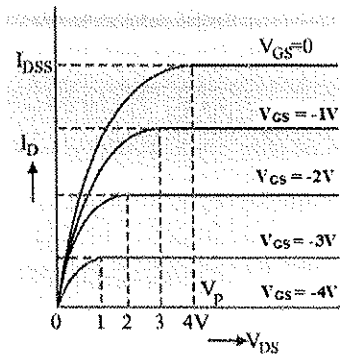


Fig. 13

3) **Cut-off region:**
As V_{GS} is made more negative for any value of V_{DS}, effective channel width decreases and at a certain value of $V_{GS} = V_P$, the channel is completely pinched-off (completely block) reducing I_D to zero for all values of V_{DS}.
For a gate-to-source voltage V_{GS} less than (more negative than) the pinch-off level, the drain current is Zero ($I_D = 0A$) as shown in Fig. 11 is called cut-off region.

Region	Function of JFET	
Saturation region	*Amplifier*	
Cut-off region	Open switch	*Switch*
Ohmic region	Closed switch	

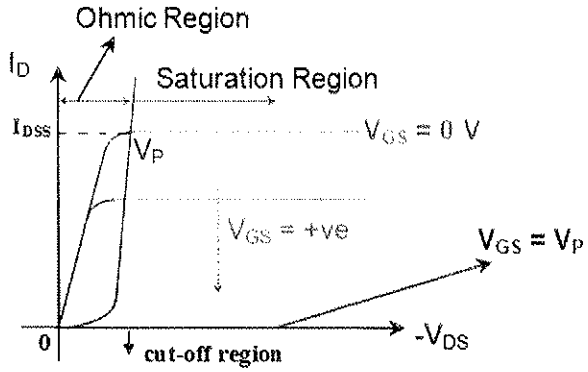


Fig. 14 drain characteristics of P-JFET

Note: *Typical p-channel JFET drain characteristics are shown in Fig. 14. It is seen that these are similar to the characteristics for an n-channel JFET, except for the voltage polarities (V_{DS} is negative). Here also when $V_{GS} = 0$ V, I_D reaches its maximum value that is I_{DSS} and progressively more positive levels of V_{GS} reduce I_D towards cut-off region.*

3.8 Transfer Characteristics of n- channel JFET:

- For the BJT transistor the output current I_C and input controlling current I_B were related by beta, which was considered constant for the analysis to be performed. In equation form,

control variable

$$I_C = f(I_B) = \beta I_B \qquad \text{----------} \rightarrow (1)$$

constant

- In Eq. (1) a linear relationship exists between I_C and I_B. Double the level of I_B and I_C will also doubles. Unfortunately, this linear relationship does not exist between the output and input quantities of a JFET.

- ***Transfer characteristics*** *are the plot of* I_D *against the variations of* V_{GS}. There is a non-linear relationship exist between I_D & V_{GS}. The relationship between I_D & V_{GS} is defined by Shockley and that equation is known as **Shockley's equation:**

control variable

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad \text{----------} \rightarrow (2)$$

constants

Where, I_{DSS} is drain to source current when gate & source are short circuited
V_P is pinch-off voltage
V_{GS} is voltage between gate & source

- In Eq. (2) I_{DSS} & V_P are constant, where as V_{GS} is control variable.
- The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed.

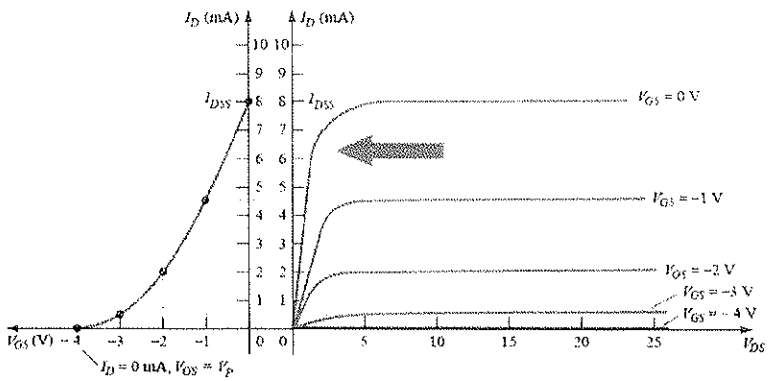


Fig. 15

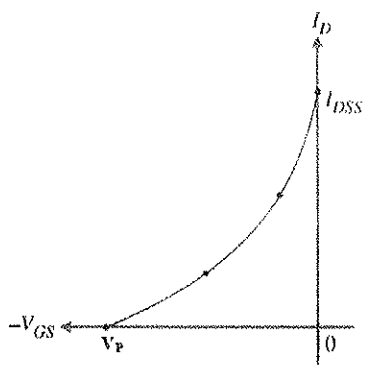


Fig. 16

- The transfer curve can be obtained using Shockley's equation or from the output characteristics.

From Eq. (2):

$$\textit{When } V_{GS}=0\ V, \quad I_D = I_{DSS}\left[1 - \frac{0}{V_P}\right]^2, \quad I_D = I_{DSS}[1-0]^2$$

Therefore,

$$I_D = I_{DSS}$$

$$\textit{When } V_{GS} = V_P, \quad I_D = I_{DSS}\left[1 - \frac{V_P}{V_P}\right]^2, \quad I_D = I_{DSS}[1-1]^2$$

Therefore,

$$I_D = 0\ mA$$

By using these two data, the transfer characteristics have been plotted that is shown in Fig. 15 & Fig.16.

From Eq. (2):

- $\frac{I_D}{I_{DSS}} = \left[1 - \frac{V_{GS}}{V_P}\right]^2$
- $\left[1 - \frac{V_{GS}}{V_P}\right] = \sqrt{\frac{I_D}{I_{DSS}}}$
- $\frac{V_{GS}}{V_P} = 1 - \sqrt{\frac{I_D}{I_{DSS}}}$
- $\boxed{V_{GS} = V_P\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]}$ ---------► (3)

- On most of the specification sheets the pinch-off voltage is specified as $V_{GS(off)}$ rather than V_P. Therefore Eq. (2) becomes

$$\boxed{I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2} \quad \text{---------►(4)}$$

Note: *For p-channel JFET Shockley's Eq. 2 can still be applied exactly as it appears. In this case, both* V_P *and* V_{GS} *will be* ***positive*** *as shown in Fig. 17 and the curve will be the mirror image of the transfer curve obtained with an n-channel.*

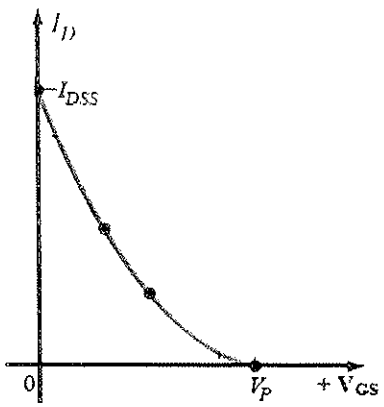


Fig. 17 Transfer curve for the p-channel JFET

3.9 Specification Sheets of JFETs:

Although the general content of specification sheets may vary from the absolute minimum to an extensive display of graphs and charts, there are a few fundamental parameters that will be provided by all manufacturers. A few of the most important are discussed in the following paragraphs. The specification sheet for the 2N5457 *n*-channel JFET as provided by Motorola is provided in Fig. 18.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	25	Vdc
Drain–Gate Voltage	V_{DG}	25	Vdc
Reverse Gate–Source Voltage	V_{GSR}	–25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	310 2.82	mW mW/°C
Junction Temperature Range	T_J	125	°C
Storage Channel Temperature Range	T_{stg}	–65 to +150	°C

Fig. 18

3.9.1 Maximum Ratings

- The maximum rating list usually appears at the beginning of the specification sheet, with the maximum voltages between specific terminals, maximum current levels, and the maximum power dissipation level of the device.
- The specified maximum levels for V_{DS} and V_{DG} must not be exceeded at any point in the design of the device.
- The applied source V_{DD} can exceed these levels, but the actual level of voltage between these terminals must never exceed the level specified. Any good design will try to avoid these levels by a good margin of safety.
- The term *reverse* in V_{GSR} defines the maximum voltage with the source positive with respect to the gate (as normally biased for an *n*-channel device) before breakdown will occur.
- On some specification sheets it is referred to as BV_{DSS} — the *B*reakdown Voltage with the Drain-Source Shorted (V_{DS} = 0 V). Although normally designed to operate with I_G = 0 mA, if *forced* to accept a gate current, it could withstand 10 mA before damage would occur.
- The total device dissipation at 25°C (room temperature) is the maximum power the device can dissipate under normal operating conditions and is defined by

$$P_D = V_{DS} I_D$$

- Gate-source cut-off voltage $V_{GS(off)} = V_P$ **is nothing but pinch-off voltage.** Another parameter is I_{DSS} (drain to source current with V_{GS}=0V) indicated on sheet. This is mentioned in the data sheet between minimum value & maximum value.

3.9.2 Operating Region

- The specification sheet and the curve defined by the pinch-off levels at each level of V_{GS} define the region of operation for linear amplification on the drain characteristics as shown in Fig. 19.
- The ohmic region defines the minimum permissible values of V_{DS} at each level of V_{GS}, and V_{DSmax} specifies the maximum value for this parameter.
- The saturation current I_{DSS} is the maximum drain current, and the maximum power dissipation level shown gives the limitation on the power dissipation in the device.
- The resulting shaded region is the normal operating region for amplifier design.

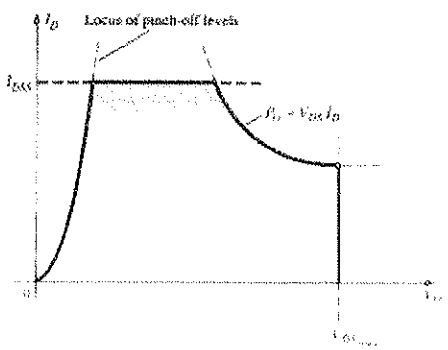


Fig. 19

JFET		BJT
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0$ A	$\Leftrightarrow$	$V_{BE} \cong 0.7$ V

Example 3.1 *Determine the value of drain current for the circuit shown below.*

Solution:

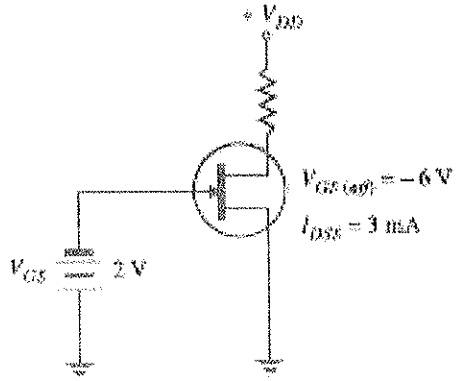
Given: V_{GS} = -2V, $V_{GS(off)}$ = -6V = V_P, I_{DSS} = 3mA

Therefore,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$I_D = (3\text{ mA})\left[\left[1 - \frac{-2}{-6}\right]^2\right]$$

$$I_D = 1.33\text{mA}$$



Example 3.2 *A JFET has the following parameters: I_{DSS} = 32mA, $V_{GS(off)}$ = - 8V & V_{GS} = - 4.5 V. Find the value of drain current.*

Solution:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$I_D = (32\text{ mA})\left[\left[1 - \frac{-4.5}{-8}\right]^2\right]$$

$$I_D = 6.12\text{mA}$$

3.10 Biasing of n - channel JFET

To use a FET in any application, (as a switch or as an amplifier) it is necessary first to bias the device. The usual reason for this biasing is to turn the device ON and operate the FET in a particular region (Saturation region or ohmic region or cut-off region) depending on the particular application.

The general relationships that can be applied to the dc analysis of all FET amplifiers are:

$$I_G \cong 0 \text{ A} \quad \text{and} \quad I_D = I_S$$

For JFETS, Shockley's equation is applied to relate the input and output quantities:

$$I_D = I_{DSS}\left(\frac{1 - V_{GS}}{V_P}\right)^2$$

3.11 Fixed-Bias Configuration (Gate Bias Configuration) for n- JFET:

- The simplest of biasing arrangement for the n-channel JFET is as shown in Fig. 20, known as fixed bias configuration.
- For AC analysis coupling capacitors C_1 & C_2 offers very low impedance and for DC analysis they offer very high impedance. Therefore open circuit C_1 & C_2.

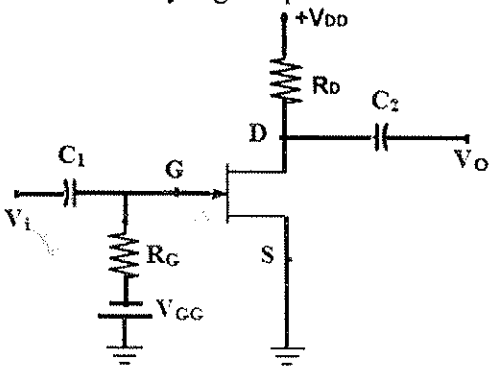


Fig. 20

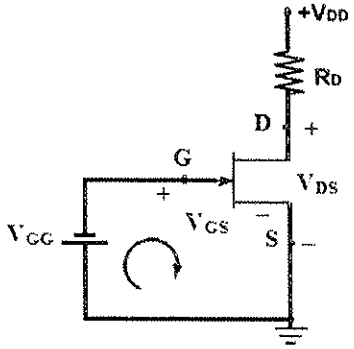


Fig. 21

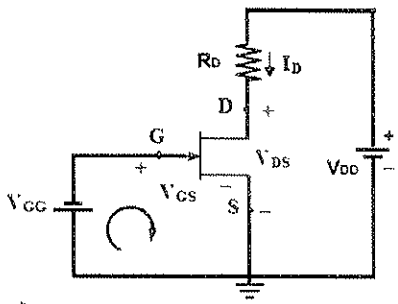


Fig. 22

- The gate resistance R_G is necessary only to isolate an AC signal.
- For the dc analysis,

$$I_G = 0 \text{ A}$$

Therefore, the voltage drop across resistance R_G is:

$$V_{RG} = I_G R_G$$
$$V_{RG} = (0) R_G$$
$$V_{RG} = 0 \text{ V}$$

- Therefore R_G is replaced by short-circuit for dc analysis. (shown in Fig. 21)
- *Apply KVL to input loop of Fig. 21*

$$-V_{GG} - V_{GS} = 0$$
$$\boxed{V_{GS} = -V_{GG}} \text{ ------} \rightarrow (5)$$

- **This biasing method is called fixed bias because the gate-to-source voltage (V_{GS}) is fixed by the constant voltage V_{GG}.**
- The network shown in Fig. 21 can be replaced by Fig. 22.
- *Apply KVL to output loop of Fig. 22*

$$V_{DD} - I_D R_D - V_{DS} = 0$$
$$\boxed{V_{DS} = V_{DD} - I_D R_D} \text{ ------} \rightarrow (6)$$

- The drain current (I_D) corresponding to V_{DS} of Eq. (2) can be obtained by Shockley's equation:

$$\boxed{I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2}$$

Merits:

- Simple biasing circuit.
- Analysis is simple.
- Design is simple.

Demerits:

- Requires two DC supplies (V_{DD} & V_{GG}), hence its use is limited.
- Thermally not stable.
- Fails to maintain the stability of Q point (operating point) against temperature & device parameter variations.

3.11.1 DC Load Line:

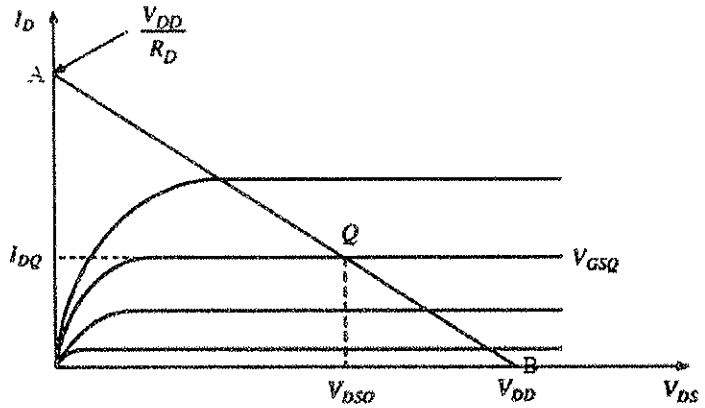


Fig. 23

Consider Eq. (6),

$$V_{DS} = V_{DD} - I_D R_D$$

From the above equation we know that,

When, $I_D = 0$,

$V_{DS} = V_{DD}$ (The load line intersects the V_{DS} axis at V_{DD}) we get a point B on X-axis

When, $V_{DS} = 0$,

$I_D = \frac{V_{DD}}{R_D}$ (The load line intersects the I_D axis at V_{DD}/R_D) we get a point A on Y-axis

The Fig. 23 shows the output characteristics of the n-channel JFET with points A & B, and line drawn between them. The line drawn between points A & B is called DC load line. The intersection of curves of different values of V_{GS} with DC load line gives **operating point or Q-point**.

The Q – point is generally situated at the middle point of the load line so that

$$V_{DSQ} = \frac{V_{DD}}{2} \text{ and } I_{DQ} = \frac{I_{DSS}}{2}$$

3.11.2 Analysis of fixed bias circuit:

Example 3.3 *For the circuit shown in the figure, calculate* V_{GSQ}, I_{DQ}, V_{DSQ} & V_D.

Solution:

From Eq. 5,

- $V_{GSQ} = -V_{GG} = -2V$

From Eq. 2,

- $I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

$I_{DQ} = (10 \times 10^{-3})\left[1 - \frac{-2}{-4}\right]^2$

$\boxed{I_{DQ} = 2.5\ mA}$

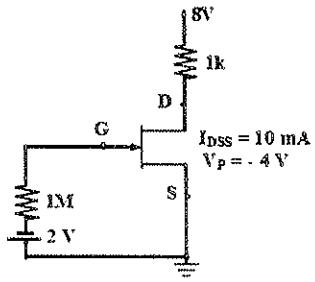
From Eq. 6,

- $V_{DSQ} = V_{DD} - I_D R_D$

$V_{DSQ} = 8 - [(2.5 \times 10^{-3}) \times (1 \times 10^3)]$

$\boxed{V_{DSQ} = 5.5\ V}$

Given:
$R_D = 1k\Omega$
$V_{DD} = 8V$
$R_G = 1M\Omega$
$V_{GG} = 2V$
$I_{DSS} = 10\ mA$
$V_P = -4V$



- $V_{DS} = V_D - V_S$

Here, $V_S = 0$ (*since source is directly connected to ground*)

$\boxed{V_{DS} = V_D = 5.5\ V}$

Example 3.4 *For the circuit shown in the figure, calculate* V_{GSQ}, I_{DQ}, V_{DSQ}, V_S, V_G & V_D.

Solution:

From Eq. 5,

- $V_{GSQ} = -V_{GG} = -2V$

From Eq. 2,

- $I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

$I_{DQ} = (10 \times 10^{-3})\left[1 - \frac{-2}{-8}\right]^2$

$\boxed{I_{DQ} = 5.625\ mA}$

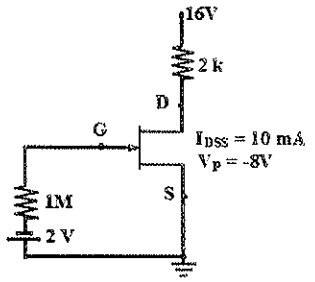
From Eq.6,

- $V_{DSQ} = V_{DD} - I_D R_D$

$V_{DSQ} = 16 - [(5.625 \times 10^{-3}) \times (2 \times 10^3)]$

$\boxed{V_{DSQ} = 4.75\ V}$

Given:
$R_D = 2\ k\Omega$
$V_{DD} = 16V$
$R_G = 1M\Omega$
$V_{GG} = 2V$
$I_{DSS} = 10\ mA$
$V_P = -8V$



- $V_{DS} = V_D - V_S$

Here, $V_S = 0$ (*since source is directly connected to ground*)

$\boxed{V_{DS} = V_D = 4.75\ V}$

- $V_{GS} = V_G - V_S$

$V_{GS} = V_G - 0$

$\boxed{V_{GS} = V_G = -2V}$

Example 3.5 *For the circuit shown in the figure, Find:* V_{DS}, I_D & V_{GG}.

Solution:

- $V_{DS} = V_D - V_S$

Here, $V_S = 0$ (*since source is directly connected to ground*)

$\boxed{V_{DS} = V_D = 9\ V}$

From Eq.6,

- $V_{DS} = V_{DD} - I_D R_D$

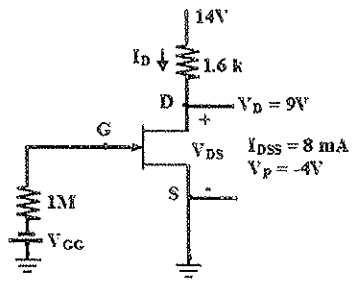
$I_D = \left[\frac{(V_{DD} - V_{DS})}{R_D}\right] = \left[\frac{14 - 9}{1.6 \times 10^3}\right] = 3.125\ mA$

$\boxed{I_D = 3.125\ mA}$

We know that, From Eq.3,

- $V_{GS} = V_P\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$

Given:
$R_D = 1.6\ k\Omega$
$V_{DD} = 14V$
$R_G = 1M\Omega$
$V_D = 9V$
$I_{DSS} = 8\ mA$
$V_P = -4V$



- $V_{GS} = -4\left[1 - \sqrt{\frac{3.125 \times 10^{-3}}{8 \times 10^{-3}}}\right]$

$\boxed{V_{GS} = -1.5\ V}$

From Eq. 5,

$\boxed{V_{GG} = -V_{GS} = 1.5V}$

3.12 Self-Bias Configuration:

- The self-bias configuration eliminates the need of two separate DC supplies. Self-bias is the most common type of biasing circuit used to bias the JFET, because it requires single DC supply for biasing (shown in Fig. 24).
- The condition required to bias the n – channel JFET is the gate-source voltage V_{GS} must be reverse biased. That is V_{GS} is negative.
- The condition required to bias the p – channel JFET is the gate-source voltage V_{GS} must be reverse biased. That is V_{GS} is positive.
- For AC analysis coupling capacitors C_1 & C_2 offers very low impedance and for DC analysis they offer very high impedance. Therefore open circuit C_1 & C_2 (shown in Fig. 25).

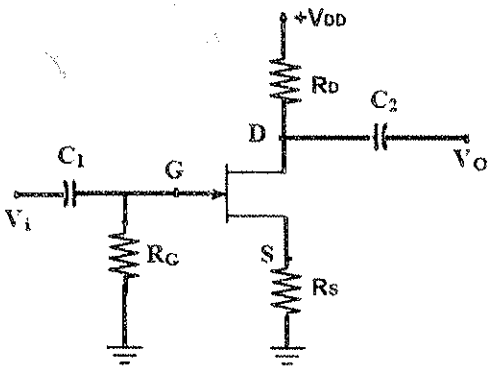


Fig. 24

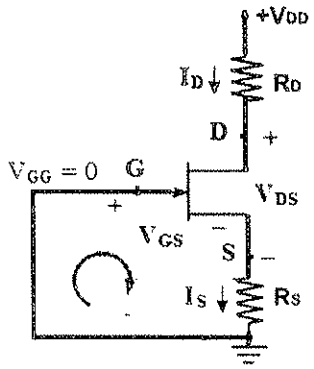


Fig. 25

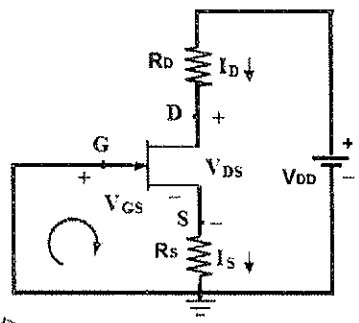


Fig. 26

- The gate Resistance R_G is necessary only to isolate an AC signal.
- For the dc analysis,

$$I_G \cong 0\ A$$

Therefore, the voltage drop across resistance R_G is:

$$V_{RG} = I_G R_G$$
$$V_{RG} = (0) R_G$$
$$V_{RG} = 0\ V$$

- Therefore R_G is replaced by short-circuit for the dc analysis. (shown in Fig. 25)
- The network shown in Fig. 25 can be replaced by Fig. 26.
- From the Fig. 26 it is observed that

$$I_D \cong I_S$$

- *Apply KVL to input loop of Fig. 26*

$$-V_{GS} - I_D R_S = 0$$
$$\boxed{V_{GS} = -I_D R_S} \text{ ------} \rightarrow (7)$$

- **Eq. (7) indicates that gate-source voltage V_{GS} is negative because of voltage drop across Rs.**
- ***The voltage drop across* Rs *makes gate-source junction reverse biased.***
- *Apply KVL to output loop of Fig. 26*

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$
But $I_D = I_S$
$$V_{DD} - I_D (R_D + R_S) - V_{DS} = 0$$
$$\boxed{V_{DS} = V_{DD} - I_D (R_D + R_S)} \text{ ----} \rightarrow (8)$$

- Shockley's equation relating input & output quantities:

$$\boxed{I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2}$$

Merits:

- Requires only one DC supply (V_{DD}) for biasing.
- Operating point (Q point) is stable against temperature variations & device parameter variations.

How resistance R_S does provide the stability against temperature & device parameter variations?

- In self bias circuit the required V_{GS} can be provided through voltage drop across resistance R_S.
- That is, $V_{GS} = - I_D R_S$ (from Eq. 7)
- When **Temperature** increases ⟶ I_D increases (because of increase in temperature more number of electrons get generated in the channel which intern increase the current I_D)
- When I_D increases ⟶ $I_D R_S$ increases (the potential drop across R_S increases)

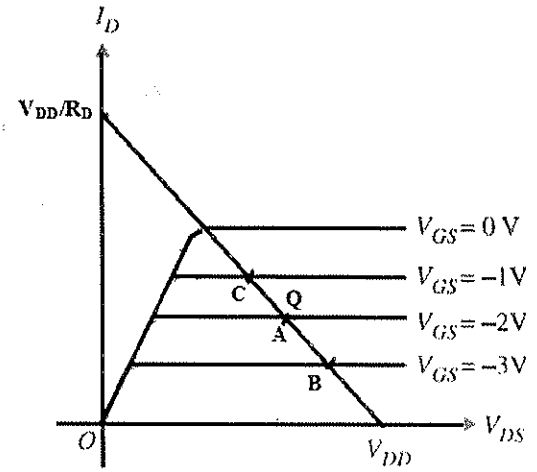


Fig. 27

- That is, $V_{GS} = - I_D R_S$ increases. (Here, the Q point depends on V_{GS}, this increase in V_{GS} causes the Q point to shift from its original position, i.e., from point A to point B, it is illustrated in Fig. 27)
- As V_{GS} increases, this makes V_{GS} more & more negative. Due to this the channel width decreases because the depletion region increases and hence **I_D decreases.** (this decrease in I_D brings the Q point to its original position, i.e., from point B to point A)
- This offsets (compensates) the initial increase in I_D.
- From the above discussion it is clear that the increasing tendency of I_D (due to rise in temperature) decreases itself. In other words there is a feedback mechanism which tends to keep I_D stable. So Q point remains stable in self bias circuit.

- Similarly,

When **temperature decreases** ⟶ **I_D decreases**

When **I_D decreases** ⟶ **$V_{GS} = - I_D R_S$ decreases**
(This decrease in V_{GS} causes the Q point to shift from its original position, i.e., from point A to point C, it is illustrated in Fig. 27)

When **V_{GS} decreases** ⟶ **I_D increases**
(As V_{GS} decreases, this makes V_{GS} less negative. Due to this the channel width increases because the depletion region decreases and hence I_D increases.

When **I_D increases** ⟶ This offsets (compensates) the initial decrease in I_D. (This increase in I_D brings the Q point to its original position, i.e., from point C to point A)

This is how the resistance R_S maintains the stability of the Q point against temperature variations, that's why this biasing circuit is called Self bias circuit.

3.12.1 Analysis of Self bias circuit:

Example 3.6 *For the circuit shown in the figure, calculate* I_{DQ}, V_{GSQ}, V_{DSQ}, V_S & V_D.

Solution: From Eq. 7,

- $V_{GS} = - I_D R_S$

From Eq. 2,

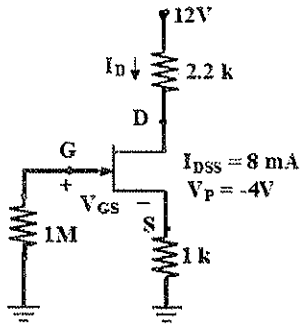
- $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$, therefore

$$I_D = I_{DSS}\left[1 - \frac{(-I_D R_S)}{V_P}\right]^2$$

$$I_D = (8 \times 10^{-3})\left[1 - \frac{(-I_D \times 1 \times 10^3)}{-4}\right]^2$$

$\boxed{I_{DQ} = 2 \text{ mA}}$

Given:
$V_{DD} = 12V$
$R_D = 2.2\ k\Omega$
$R_G = 1M\Omega$
$R_S = 1\ k\Omega$
$I_{DSS} = 8\ mA$
$V_P = -4V$



Therefore,

- $V_{GS} = - I_D R_S$

$V_{GS} = - (2 \times 10^{-3} \times 1 \times 10^3)$

$\boxed{V_{GSQ} = - 2 \text{ V}}$

From Eq. 8,

- $V_{DS} = V_{DD} - I_D (R_D + R_S$

$V_{DS} = 12 - (2 \times 10^{-3})[(2.2 \times 10^3) + (1 \times 10^3)]$

$\boxed{\mathbf{V_{DSQ} = 5.6 \text{ V}}}$

- $V_S = I_D R_S$

$V_S = (2 \times 10^{-3})(1 \times 10^3)$

$V_S = 2 \text{ V}$

- $V_{DS} = V_D - V_S$

$V_D = V_{DS} + V_S$

$V_D = 5.6 + 2$

$\boxed{\mathbf{V_D = 7.6 \text{ V}}}$

Example 3.7 *Given* $V_S = 1.7$ V *for the network of figure below. Find* I_{DQ}, V_{GSQ}, I_{DSS}, V_D & V_{DS}.

Solution:

We know that,

- $V_S = I_D R_S$

$$I_D = \frac{V_S}{R_S} = \frac{1.7}{0.51 \times 10^3} = \mathbf{3.34\ mA}$$

From Eq. 7,

- $V_{GS} = - I_D R_S$

$V_{GS} = -(3.34 \times 10^{-3} \times 0.51 \times 10^3)$

$\boxed{V_{GSQ} = -1.7 \text{ V}}$

From Eq. 2,

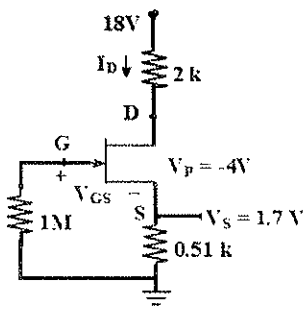
- $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$,

Therefore,

$$(3.34 \times 10^{-3}) = I_{DSS}\left[1 - \frac{(-1.7)}{-4}\right]^2$$

$\boxed{\mathbf{I_{DSS} = 10.11\ mA}}$

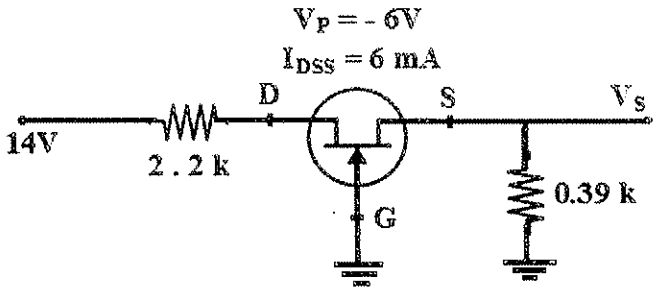
Given:
$V_{DD} = 18V$
$R_D = 2\ k\Omega$
$R_G = 1M\Omega$
$R_S = 0.51\ k\Omega$
$V_P = -4V$
$V_S = 1.7$ V



From Eq. 8,

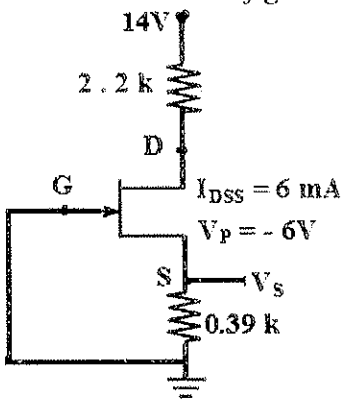
- $V_{DS} = V_{DD} - I_D (R_D + R_S)$
  $V_{DS} = 18 - (3.34 \times 10^{-3})[(2 \times 10^3) + (0.51 \times 10^3)]$
  $\boxed{V_{DS} = 9.62\ V}$
- $V_{DS} = V_D - V_S$
  $V_D = V_{DS} + V_S$
  $V_D = 9.62 + 1.7$
  $\boxed{V_D = 11.32\ V}$

Example 3.8 Find V_S for *the circuit shown in figure.*



Solution:

The given circuit is redrawn as shown in the figure below



Given
$V_{DD} = 14V$
$R_D = 2.2\ k\Omega$
$R_S = 0.39\ k\Omega$
$V_P = -6V$
$I_{DSS} = 6$ mA

From Eq. 7,

- $V_{GS} = -I_D R_S$
  $V_{GS} = -I_D \times (0.39 \times 10^3)$

From Eq. 2 ,

- $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$.

Therefore,

$$I_D = I_{DSS}\left[1 - \frac{(-I_D R_S)}{V_P}\right]^2$$

$$I_D = (6 \times 10^{-3})\left[1 - \frac{(-I_D \times 0.39 \times 10^3)}{-6}\right]^2$$

$\boxed{I_D = 3.56\ mA}$

- $V_S = I_D R_S$
  $V_S = (3.56 \times 10^{-3})(0.39 \times 10^3)$
  $\boxed{V_S = 1.39\ V}$

3.13 VOLTAGE-DIVIDER BIAS CONFIGURATION:

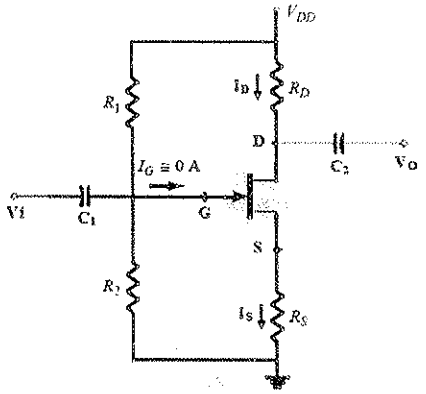


Fig. 28

- Fig. 28 shows the voltage divider bias circuit for n – channel JFET.
- We know that Gate current, $I_G = 0$ for JFET.
- For DC analysis network of Fig. 28 can be redrawn as shown in Fig. 29 & Fig. 30. Here, coupling capacitors are replaced by open circuit.
- V_{DD} can be treated as separate two sources.
- Here, from Fig. 30

  $I_{R1} = I_{R2} + I_G$

  since $I_G = 0$

  $I_{R1} = I_{R2}$
- Same current is flowing through R_1 & R_2, therefore they are in series.
- Here, V_G is voltage between gate and ground.
- The voltage V_G is given by
- $V_{R2} = V_G = I_{R2}R_2$

$$I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$

Therefore,

$$V_G = \frac{V_{DD}\, R_2}{R_1 + R_2} \dashrightarrow \quad (9)$$

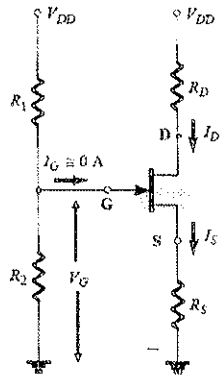


Fig. 29

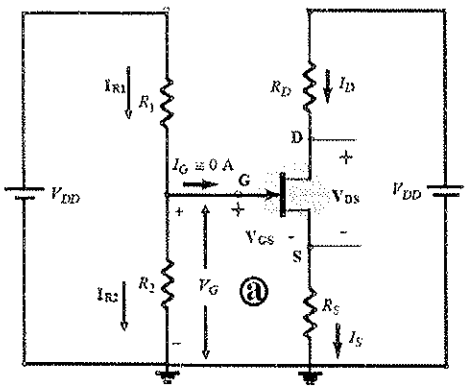


Fig. 30

- Apply KVL around loop a to the Fig. 30

  $V_G - V_{GS} - I_D R_S = 0$

  $V_{GS} = V_G - I_D R_S \dashrightarrow \quad (10)$

- Apply KVL around output loop of Fig. 30

  $V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$

  $V_{DS} = V_{DD} - I_D(R_D + R_S) \dashrightarrow \quad (11)$

- Shockley's equation relating input and output quantities is:

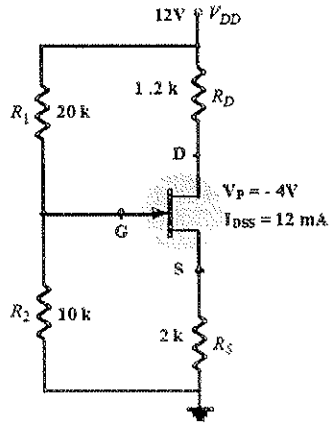
$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

3.13.1 Analysis of Voltage-Divider Bias Configuration:

Example 3.9 *For the circuit shown in the figure below, calculate* V_G, I_D, V_{GS}, V_{DS} & V_S.

Solution:

Given:
$V_{DD} = 12V$
$V_P = -4V$
$I_{DSS} = 12$ mA
$R_1 = 20$ kΩ
$R_2 = 10$ kΩ
$R_D = 1.2$ kΩ
$R_S = 2$ kΩ



From Eq. 9,

- $V_G = \frac{V_{DD} R_2}{R_1 + R_2}$

  $V_G = \frac{12 \times 10 \times 10^3}{(20 \times 10^3) + (10 \times 10^3)}$

  $\mathbf{V_G = 4V}$

- $V_{GS} = V_G - I_D R_S$

  $V_{GS} = 4 - (I_D \times 2 \times 10^3)$

From Eq. 2,

- $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

  Therefore,

  $I_D = I_{DSS}\left[1 - \frac{(4 - I_D R_S)}{V_P}\right]^2$

  $I_D = (12 \times 10^{-3}) \left[1 - \frac{(4 - (I_D \times 2 \times 10^3))}{-4}\right]^2$

  $\mathbf{I_D = 3\ mA}$

From Eq. 11,

- $V_{DS} = V_{DD} - I_D (R_D + R_S)$

  $V_{DS} = 12 - (3 \times 10^{-3})[(1.2 \times 10^3) + (2 \times 10^3)]$

  $\mathbf{V_{DS} = 2.4\ V}$

Therefore,

- $V_{GS} = V_G - I_D R_S$

  $V_{GS} = 4 - (3 \times 10^{-3} \times 2 \times 10^3)$

  $\mathbf{V_{GS} = -2\ V}$

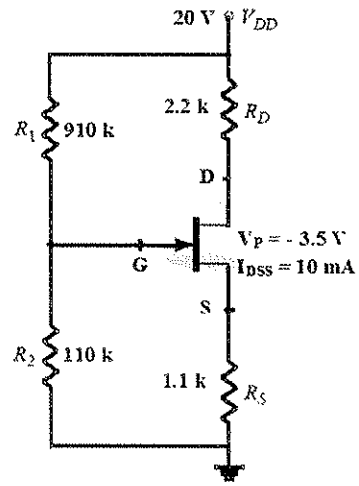
- $V_S = I_D R_S$

  $V_S = (3 \times 10^{-3})(2 \times 10^3)$

  $\mathbf{V_S = 6\ V}$

Example 3.10 *For the circuit shown in the figure below, calculate* V_G, I_{DQ}, V_{GSQ}, V_D, V_S & V_{DSQ}.

Solution:



Given:
$V_{DD} = 20$ V
$V_P = -3.5$ V
$I_{DSS} = 10$ mA
$R_1 = 910$ kΩ
$R_2 = 110$ kΩ
$R_D = 2.2$ kΩ
$R_S = 1.1$ kΩ

From Eq. 9,

- $V_G = \dfrac{V_{DD} R_2}{R_1 + R_2}$

  $V_G = \dfrac{20 \times 110 \times 10^3}{(910 \times 10^3) + (110 \times 10^3)}$

  $V_G = \mathbf{2.16\ V}$

- $V_{GS} = V_G - I_D R_S$

  $V_{GS} = 2.16 - (I_D \times 1.1 \times 10^3)$

From Eq. 2,

- $I_D = I_{DSS}\left[1 - \dfrac{V_{GS}}{V_P}\right]^2$,

  Therefore,

  $I_D = (10 \times 10^{-3}) \left[1 - \dfrac{(2.16 - (I_D \times 1.1 \times 10^3))}{-3.5}\right]^2$

  $\mathbf{I_D = 3.32\ mA}$

Therefore,

- $V_{GS} = V_G - I_D R_S$

  $V_{GS} = 2.16 - (3.32 \times 10^{-3} \times 1.1 \times 10^3)$

  $\mathbf{V_{GS} = -1.492\ V}$

From Eq. 11,

- $V_{DS} = V_{DD} - I_D (R_D + R_S)$

  $V_{DS} = 20 - (3.32 \times 10^{-3})[(2.2 \times 10^3) + (1.1 \times 10^3)]$

  $\mathbf{V_{DS} = 9\ V}$

- $V_S = I_D R_S$

  $V_S = (3.32 \times 10^{-3})(1.1 \times 10^3)$

  $\mathbf{V_S = 3.652\ V}$

- $V_{DS} = V_D - V_S$

  Therefore,

  $V_D = V_{DS} + V_S$

  $V_D = 9 + 3.652$

  $\mathbf{V_D = 12.652\ V}$

FET Small Signal Analysis

4.1 Introduction:

- Field-effect transistor (JFET) amplifiers provide an excellent voltage gain with the added feature of high input impedance. Because of their high input impedance and other characteristics features of JFETs, they are preferred over BJTs for certain types of applications.
- Whereas a BJT device controls a large output (collector) current by means of a relatively small input (base) current, the FET device controls an output (drain) current by means of a small input (gate-source voltage) voltage.
- In general, therefore, the BJT is a current-controlled device and the FET is a voltage-controlled device. In both cases, however, note that the output current is the controlled variable.
- Because of the high input characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs. While the BJT had an amplification factor, β (beta), the FET has a transconductance factor, g_m.
- There are three terminals in a JFET viz., source, gate and drain. However, when JFET is to be connected in a circuit, we require four terminals; two for the input and two for the output. This difficulty is overcome by making one terminal of the JFET common to both input and output terminals.
- Accordingly, a JFET can be connected in a circuit in the following three ways (configurations):
    1) Common source (CS) configuration
    2) Common drain (CD) configuration
    3) Common gate (CG) configuration
- The common source connection is the most widely used arrangement. It is because this connection provides high input impedance, good voltage gain and moderate output impedance. However, the circuit produces a phase reversal i.e., output signal is 180° out of phase with the input signal.
- A common source JFET amplifier is the JFET equivalent of common emitter amplifier. Both amplifiers have a 180° phase shift from input to output. Although the two amplifiers serve the same basic purpose, the means by which they operate are quite different.

4.2 Basic CS configuration amplifier:

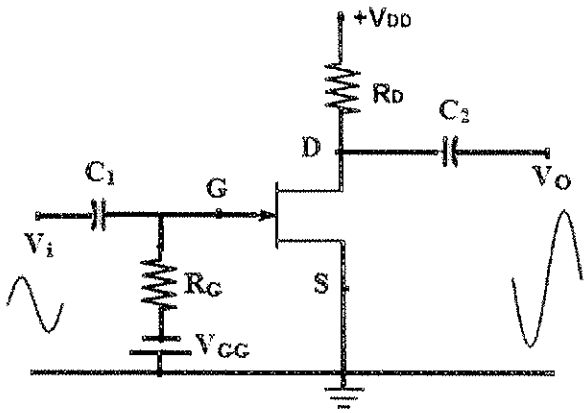


Fig. 1 common source circuit

- Fig.1 shows a common source n-channel JFET fixed bias amplifier. Note that source terminal is common to both input and output.
- In Fig.1, the voltage V_{GG} provides the necessary reverse bias between gate and source of the JFET. The Input AC signal to be amplified is applied between gate and source through coupling capacitor C_1.

- V_{DD} is another DC supply to bias drain and source. Output voltage V_0 can be obtained through another coupling capacitor C_2 between drain and source of JFET.

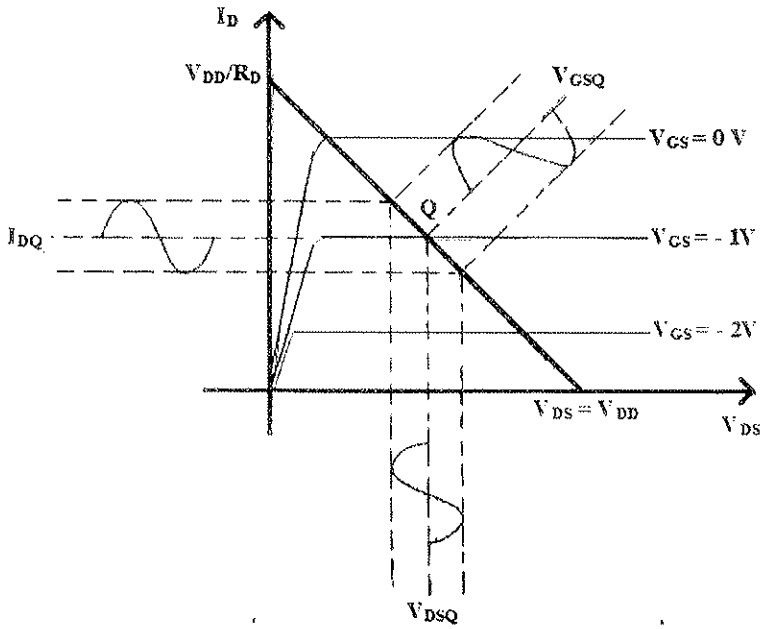


Fig. 2 Output characteristics of n-channel JFET

- Drain characteristics of JFET is as shown in Fig. 2.
  Apply KVL to output circuit of Fig. 1

$$V_{DS} = V_{DD} - I_D R_D \text{ ----------} \rightarrow \quad (1)$$ (Eq. 1 represents straight line)

when, $I_D = 0$; $V_{DS} = V_{DD}$ point on X-axis

when, $V_{DS} = 0$; $I_D = \frac{V_{DD}}{R_D}$ point on Y- axis

- Q-point is selected approximately at the midpoint of the load line. This gives undistorted output, i.e., output waveform is sinusoidal when the input signal applied is sinusoidal. This is valid when input signal is small at lower frequency and operating in the linear region.
- If the operating point is selected either close to the ohmic region or near the cut-off region that is at the one of the ends of the load line, the output sinusoidal would be clipped during either the positive or negative half-cycles of the input signal.

4.3 FET Small - Signal Model:

- The ac analysis of an FET configuration requires that a small-signal ac model for the FET. The gate to source voltage V_{GS} controls the drain to source current I_D of an FET.
- The relationship between V_{GS} and I_D is given by Shockley's equation.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \text{ ----------} \rightarrow \quad (2)$$

- The drain current is controlled by the gate – source voltage (V_{GS}).

i.e., $I_D = f(V_{GS})$

$I_D \propto V_{GS}$

$$I_D = g_m V_{GS} \text{ ----------} \rightarrow \quad (3)$$

Here, g_m is called the transconductance of FET.

g_m is alternatively represented by y_{fs}. therefore,

$$g_m = y_{fs} \text{ ----------} \rightarrow \quad (4)$$

Here, y_{fs} is called forward transfer admittance.

4.3.1 Transconductance (g_m):

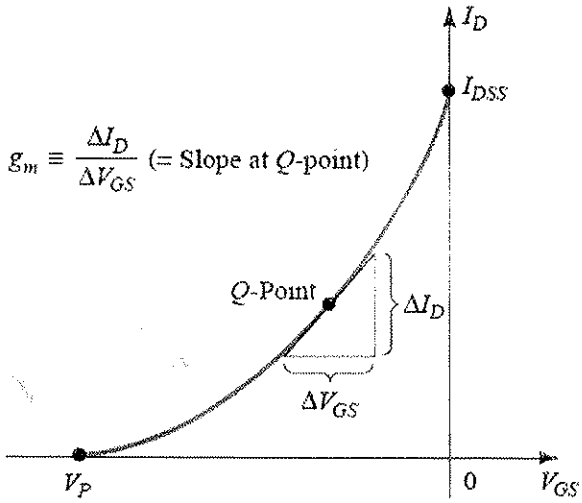


Fig. 3

- The transconductance g_m of an FET can be defined as the change in drain current that will result from a change in gate to source voltage with drain to source voltage remains constant.
- $g_m = \frac{\text{Change in } I_D}{\text{Change in } V_{GS}}$, its unit is Siemens (S) or mho

Therefore,

- $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ ----→ (5)
- Transconductance can be determined from transfer characteristics as shown in Fig. 3.
- Select Q point on the transfer characteristics and draw tangent at the Q point.
- Small change in drain current to small change in V_{GS} about Q point gives gm.

Mathematical expression of g_m:

- Consider Eq. 2

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \text{ ----------} \rightarrow (2)$$

- Differentiate Eq. 2 w. r. t., V_{GS} we get,

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \right]$$

$$= I_{DSS}\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 2I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$= 2I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)\left[\frac{d}{dV_{GS}}(1) - \frac{1}{V_P}\frac{dV_{GS}}{dV_{GS}}\right]$$

$$= 2I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)\left(0 - \frac{1}{V_P}\right)$$

$$\boxed{g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right)} \text{ ----------} \rightarrow (6)$$

- Where, $|V_P|$ denotes magnitude only, to ensure positive value for g_m. Because, g_m is forward transfer admittance.

- When $V_{GS} = 0$ V, the Eq. 6 becomes:

$$g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{0}{V_P}\right)$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} \text{ ----------} \rightarrow (7)$$

Where, added subscript 0 reminds us that it is the value of g_m when $V_{GS} = 0$V.
Therefore, Eq. 6 then becomes

$$\boxed{g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right)} \text{ ----------} \rightarrow (8)$$

Example 4.1 *For JFET, if* I_{DSS} = 10 mA, V_P = - 5V and g_{m0} = 4mS. *Determine the transconductance for* V_{GS} = - 4V *and find* I_D *at this point.*

Solution:

Given:
I_{DSS} = 10 mA
V_P = -5V
V_{GS} = -4V
g_{m0} = 4mS

From Eq. 8

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$g_m = (4 \times 10^{-3})\left(1 - \frac{-4}{-5}\right)$$

$$\mathbf{g_m = 0.8\ mS}$$

From Eq. 2

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$I_D = (10 \times 10^{-3})\left[1 - \frac{-4}{-5}\right]^2$$

$$\mathbf{I_D = 0.4\ mA}$$

Example 4.2 For *JFET, if* I_{DSS}= 8 mA, V_P= - 4V *find: (a) The transconductance at* V_{GS} = 0V
(b) The transconductance when V_{GS} = - 0.5V
(c) Calculate drain current I_D at V_{GS} = - 0.5V

Solution:

Given:
I_{DSS} = 8 mA
V_P = - 4V

Transconductance at V_{GS} = 0V is g_{m0}
Therefore, From Eq. 7

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

$$= \frac{2 \times 8 \times 10^{-3}}{4}$$

$$\mathbf{g_{m0} = 4\ mS}$$

The transconductance when V_{GS} = - 0.5V is

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$g_m = (4 \times 10^{-3})\left(1 - \frac{-0.5}{-4}\right)$$

$$\mathbf{g_m = 3.5\ mS}$$

From Eq. 2

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$I_D = (8 \times 10^{-3})\left[1 - \frac{-0.5}{-4}\right]^2$$

$$\mathbf{I_D = 6.125\ mA}$$

4.3.2 FET input impedance Z_i :

The input impedance of all commercially available FETs is sufficiently large. Therefore input terminals of FET can be treated as an open circuit.

Since I_G = 0A,

$$Z_i = \frac{V_i}{I_G} = \frac{V_i}{0}$$

$$\boxed{Z_i = \infty}$$

4.3.3 FET output impedance Z_O :

- Drain to source resistance (r_d) is the resistance between the drain and source terminals when the JFET is operated in saturation region.
- It is the ratio of change in drain to source voltage (ΔV_{DS}) to the change in drain current (ΔI_D) at constant gate source voltage.
- r_d ⟶ resistance from drain to source

Therefore,

$$r_d = \frac{V_{DS2} - V_{DS1}}{I_{D2} - I_{D1}}$$

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$$

- Output impedance of the FET is:

$$Zo = r_d$$

- Since r_d is usually the output resistance of a JFET it may also be expressed as output admittance y_{os}. (on FET specification sheet the output impedance will typically appear as admittance parameter y_{os})

y_{os} ⟶ admittance equivalent at output terminal with respect to source

Therefore,

$$\boxed{Zo = r_d = \frac{1}{y_{os}}} \text{ ----------} \rightarrow (9)$$

- Referring to the output characteristics of a JFET in Fig. 4 it is clear that above the pinch-off voltage, the change in I_D (I_{D1} to I_{D2}) is small for a change in V_{DS} (V_{DS1} to V_{DS2}) because the curve is almost flat. Therefore, drain resistance of a JFET has a large value ranging from **10 kΩ to 1 MΩ.**

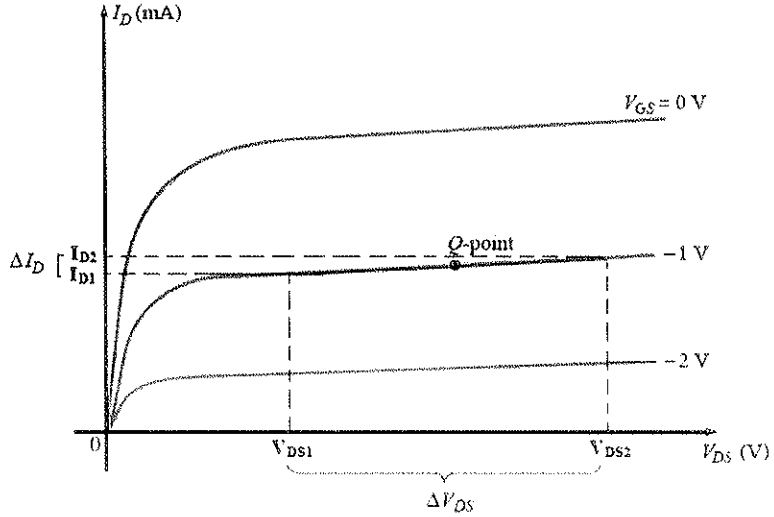


Fig. 4

4.3.4 Amplification factor:

- Amplification factor is the ratio of change in output voltage to the change in input voltage when drain current remains constant.

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \quad \text{at constant } I_D$$

$$\mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\boxed{\mu = r_d g_m} \text{ ----------} \rightarrow (10)$$

4.3.5 Impact of I_D on g_m:

- A mathematical relationship between g_m and I_D can be derived by noting that Shockley's equation can be written in the following form:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \text{ ----} \rightarrow \frac{I_D}{I_{DSS}} = \left[1 - \frac{V_{GS}}{V_P}\right]^2 \text{ ----} \rightarrow \left[1 - \frac{V_{GS}}{V_P}\right] = \sqrt{\frac{I_D}{I_{DSS}}}$$

but $g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right)$

$$\boxed{g_m = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}} \text{ --------} \rightarrow (11)$$

4.4 FET AC Equivalent Circuit:

The small signal ac model of FET is required in the ac analysis of FET amplifiers. The small signal ac model is developed using the following facts.

- The input impedance between gate and source terminals of an FET is very high (since $I_G = 0$). Therefore FET can be represented by an open circuit at the input terminal G and S.
- The output impedance is represented by the resistor r_d from drain to source.
- The control of I_D by V_{gs} is included as a current source $g_m V_{gs}$ connected from drain to source as shown in Fig. 5.
- The current source $g_m V_{gs}$ is voltage controlled that is controlled by input voltage V_{gs} applied between input terminal G and S. The current source has its arrow pointing from drain to source to establish an 180^0 phase shift between output and input voltages.
- The lower case suffixes are used to imply that V_{gs}, g_m and r_d are all ac values.

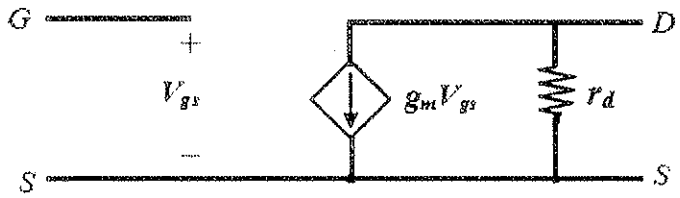


Fig. 5

Example 4.3 *An FET has* y_{fs}=3.8 mS and y_{os}= 20 µS. *Find* g_m *and* r_d

Solution:

- $g_m = y_{fs} = 3.8$ mS
- $r_d = \frac{1}{y_{os}} = \frac{1}{20\times10^{-6}}$

  $r_d = 50$ kΩ

4.5 JFET Common Source Amplifier Using Fixed bias Configuration:

- The fixed bias CS amplifier with input voltage Vi applied through coupling capacitor C_1 and connected to output through another coupling capacitor C_2 is shown in Fig. 6.
- The analysis of JFET CS amplifier for its small signal behavior can be made by following simple guidelines:

Guide line 1: Draw the actual circuit diagram.

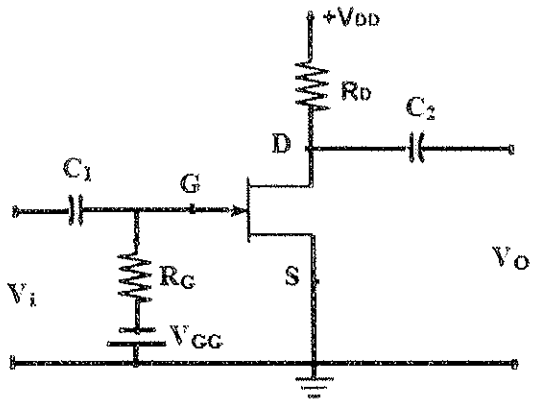


Fig. 6

Guide line 2: Replace Coupling capacitors and bypass capacitor with short circuit. (Because the capacitors are selected in such a way that they should offer very less reactance to the AC)

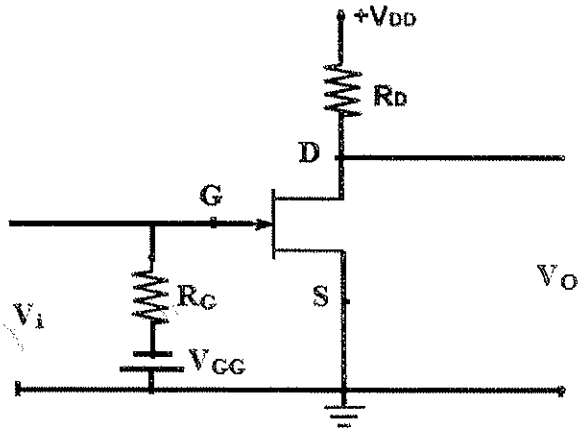


Fig. 7

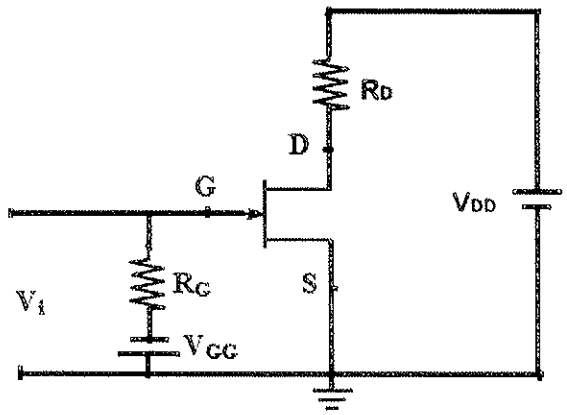


Fig.8

Guide line 3: Replace all the DC sources (V_{DD} & V_{GG}) with short circuit.

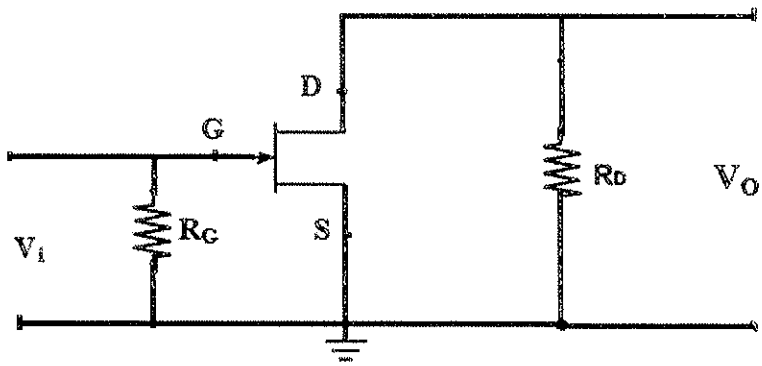


Fig. 9

Guide line 4: Replace FET terminals Gate (G), Drain (D) and Source (S) with its equivalent circuit.

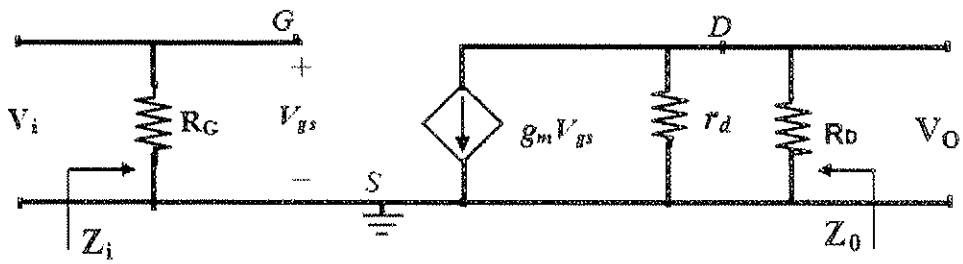


Fig. 10

4.5.1 Input Impedance (Z_i):

Fig. 10 clearly reveals that, there is an open circuit between the gate and source terminals; hence the input impedance is nothing but R_G.

Therefore,

$$\boxed{Z_i = R_G} \quad \text{----------} \rightarrow (12)$$

4.5.2 Output Impedance (Z_o):

- To find the output impedance we have to set Vi to zero. ($V_i = 0$)
- From the Fig. 10 it is observed that $V_i = V_{gs}$.
- Hence, with Vi = 0, $g_m V_{gs} = 0$.
- Thus the current source $g_m V_{gs}$ is represented by an open circuit as shown in Fig. 11.
- From the circuit of Fig. 11, the output impedance Z_o is given by:

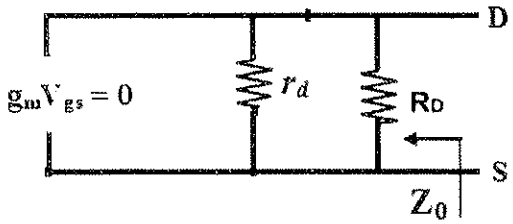


Fig. 11

$$\boxed{Z_o = r_d \,||\, R_D} \dashrightarrow (13)$$

$$Z_o = \frac{R_D r_d}{R_D + r_d}$$

- If the resistance r_d is sufficiently large (at least 10:1) compared to R_D, (i.e., $r_d >= 10R_D$), the approximation $(r_d \,||\, R_D) \approx R_D$ can often be applied.
- Therefore, $Z_o \approx R_D$

4.5.3 Voltage gain (A_V):

- $A_v = \frac{V_O}{V_i} = \frac{\text{output voltage}}{\text{input voltage}}$

From Fig. 10

$$V_i = V_{gs}$$

The output circuit of Fig. 10 is redrawn in Fig. 12 for convenience.

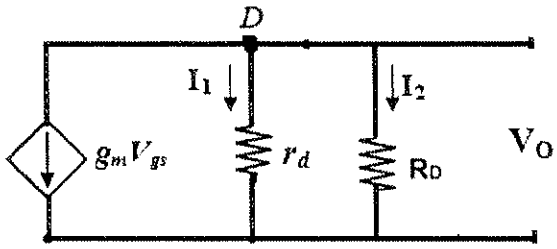


Fig. 12

Apply KCL to node D, we have

- $g_m V_{gs} + I_1 + I_2 = 0$

Here, $I_1 = \frac{V_O}{r_d}$ and $I_2 = \frac{V_O}{R_D}$

Therefore,

- $g_m V_{gs} + \frac{V_O}{r_d} + \frac{V_O}{R_D} = 0$
- $\frac{V_O}{r_d} + \frac{V_O}{R_D} = - g_m V_{gs}$
- $V_O \left[\frac{1}{r_d} + \frac{1}{R_D}\right] = - g_m V_{gs}$
- $V_O \left[\frac{r_d + R_D}{r_d R_D}\right] = - g_m V_{gs}$
- $V_O = - g_m V_{gs} \left[\frac{r_d R_D}{r_d + R_D}\right]$
- $V_O = - g_m V_{gs} (r_d \,||\, R_D)$

Therefore,

- $A_v = \frac{V_O}{V_i} = \frac{- g_m V_{gs} (r_d \,||\, R_D)}{V_{gs}}$
- $\boxed{A_V = - g_m (r_d \,||\, R_D)} \dashrightarrow (14)$

- The negative sign in the above equation clearly reveals a phase shift of 180^0 between input and output voltages.
- If $r_d \geq 10 R_D$

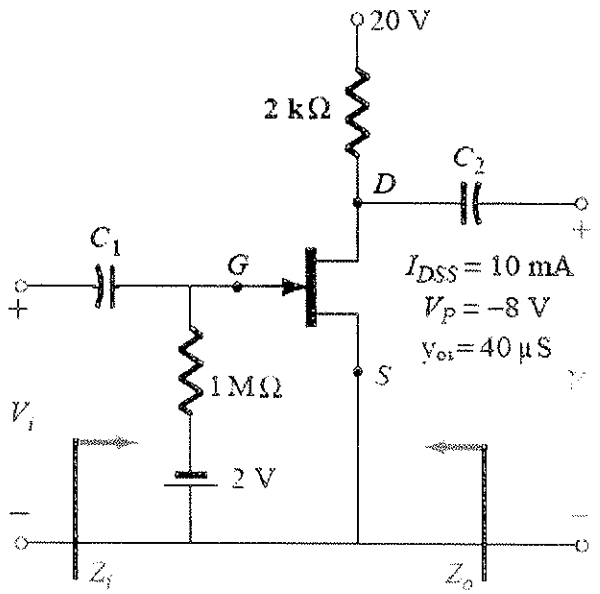
$$\boxed{A_V = - g_m R_D}$$

Example 4.4 *For the FET amplifier shown below: Find* g_m, r_d, Z_i, Z_o, A_V and A_V by ignoring the effect of r_d.

Solution:

Given :

$V_{GG} = 2$ V
$I_{DQ} = 5.625$ mA
$I_{DSS} = 10$ mA
$V_P = -8$ V
$R_G = 1$ MΩ
$R_D = 2$ kΩ
$V_{DD} = 20$ V
$y_{os} = 40$ μS



For fixed bias circuit, We know that:

$V_{GS} = -V_{GG}$

$V_{GS} = -2$ V

- $g_{m0} = \frac{2I_{DSS}}{|V_P|}$

$= \frac{2\times10\times10^{-3}}{8}$

$g_{m0} = 2.5$ mS

- $g_m = g_{mo}(1 - \frac{V_{GS}}{V_P})$

$= (2.5\times10^{-3})(1 - \frac{-2}{-8})$

$g_m = 1.88$ mS

- $Z_0 = (r_d \,||\, R_D) = \frac{R_D r_d}{R_D + r_d}$

$= \frac{(2\times10^3)(25\times10^3)}{(2\times10^3)+(25\times10^3)}$

$Z_0 = 1.85$ kΩ

- $r_d = \frac{1}{y_{os}} = 25$ kΩ
- $Z_i = R_G = 1$ MΩ
- $A_V = -g_m(r_d \,||\, R_D)$
  $= -(1.88\times10^{-3})(1.85\times10^3)$
  $A_V = -3.4$
- $A_V = -g_m R_D$
  $= -(1.88\times10^{-3})(2\times10^3)$
  $A_V = -3.76$

Example 4.5 *For the FET amplifier shown below:*

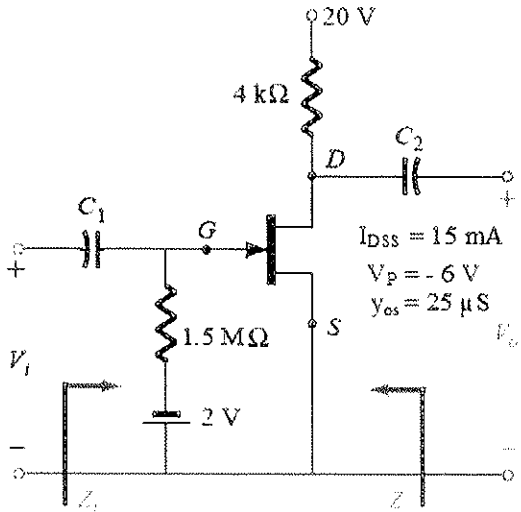
a) Calculate Z_i, Z_o & A_V

b) Calculate Z_i, Z_o & A_V, by neglecting the effect of r_d and compare the results.

Solution:

Given :

$I_{DSS} = 15$ mA
$V_P = -6$ V
$y_{os} = 25$ μS
$R_G = 1.5$ MΩ
$R_D = 4$ kΩ
$V_{GG} = 2$ V
$V_{DD} = 20$ V



a)

For fixed bias circuit, We know that:

$V_{GS} = -V_{GG}$

$V_{GS} = -2$ V

- $g_{m0} = \frac{2I_{DSS}}{|V_P|}$

$= \frac{2\times15\times10^{-3}}{6}$

$g_{m0} = 5$ mS

- $g_m = g_{mo}(1 - \frac{V_{GS}}{V_P})$

  $= (5\times10^{-3})(1 - \frac{-2}{-6})$

  $\mathbf{g_m = 3.33\ mS}$

- $Z_0 = (r_d \,||\, R_D) = \frac{R_D r_d}{R_D + r_d}$

  $= \frac{(4\times10^3)(40\times10^3)}{(4\times10^3)+(40\times10^3)}$

  $\mathbf{Z_0 = 3.63\ k\Omega}$

- $r_d = \frac{1}{Y_{OS}} = (1/(25\times10^{-6})) = \mathbf{40\ k\Omega}$
- $\mathbf{Z_i = R_G = 1.5\ M\Omega}$
- $A_V = -g_m(r_d \,||\, R_D)$

  $= -(3.33\times10^{-3})(3.63\times10^3)$

  $\mathbf{A_V = -12.08}$

b) Since $r_d = 10\ R_D$, we can ignore the effect of r_d. Therefore we have,

- $\mathbf{Z_i = R_G = 1.5\ M\Omega}$
- $\mathbf{Z_o = R_D = 4\ k\Omega}$
- $A_V = -g_m R_D$

  $= -(3.33\times10^{-3})(4\times10^3)$

  $\mathbf{A_V = -13.32}$

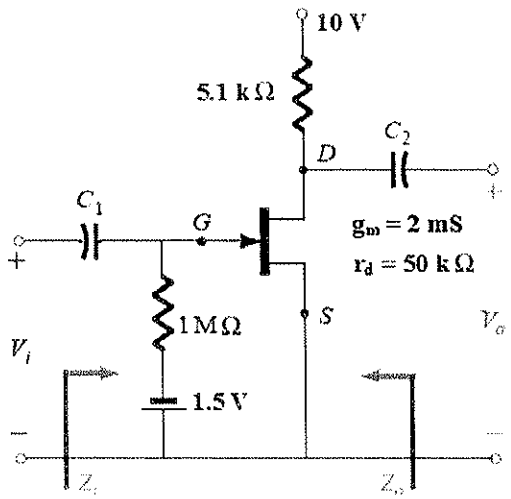
The results are compared in the following table

Parameter	With r_d	Without r_d
Z_i	1.5 MΩ	1.5 MΩ
Z_o	3.63 kΩ	4 kΩ
A_V	-12.08	- 13.32

It is observed from the above table that both the results are approximately equal.

Example 4.6 *For the FET amplifier shown below: Calculate* Z_i, Z_o & A_V.

Solution:



Given :

$V_{GG} = 1.5$ V
$V_{DD} = 10$ V
$r_d = 50$ kΩ
$R_G = 1$ MΩ
$R_D = 5.1$ kΩ
$g_m = 2$ mS

For fixed bias circuit, We know that:

$V_{GS} = -V_{GG}$

$V_{GS} = -1.5$ V

- $\mathbf{Z_i = R_G = 1\ M\Omega}$
- $Z_0 = (r_d \,||\, R_D) = \frac{R_D r_d}{R_D + r_d}$

  $= \frac{(5.1\times10^3)(50\times10^3)}{(5.1\times10^3)+(50\times10^3)}$

  $\mathbf{Z_0 = 4.628\ k\Omega}$

- $A_V = -g_m(r_d \,||\, R_D)$

  $= -(2\times10^{-3})(4.628\times10^3)$

  $\mathbf{A_V = -9.256}$

4.6 JFET Common Source Amplifier Using Self-bias Configuration (with bypassed R_S) :

- The self-bias CS amplifier with input voltage Vi applied through coupling capacitor C_1 and connected to output through another coupling capacitor C_2 is shown in Fig. 13.
- The analysis of JFET CS amplifier for its small signal behavior can be made by following simple guidelines:

Guide line 1: Draw the actual circuit diagram.

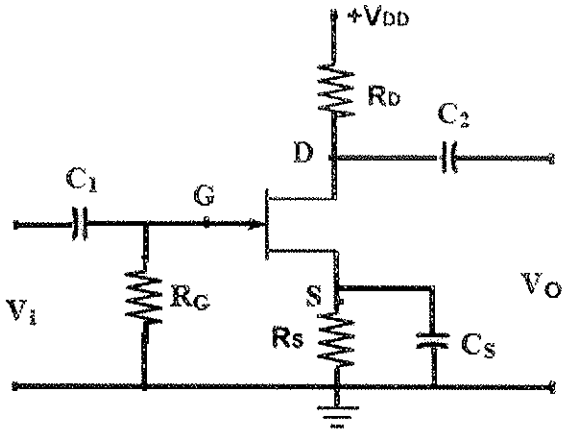


Fig. 13

Guide line 2: Replace Coupling capacitors and bypass capacitor with short circuit. (Because the capacitors are selected in such a way that they should offer very less reactance to the AC)

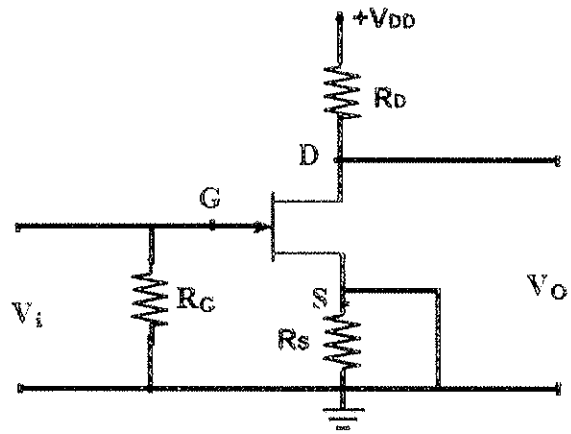


Fig. 14

From the Fig. 15 it is observed that, after short circuiting coupling capacitor CS, the resistance R_S is in parallel with zero ohms. So their parallel combination is also zero. Therefore, resistance R_S in Fig. 14 can be replaced with 0 Ω as shown in Fig. 16.

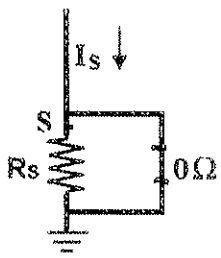


Fig. 15

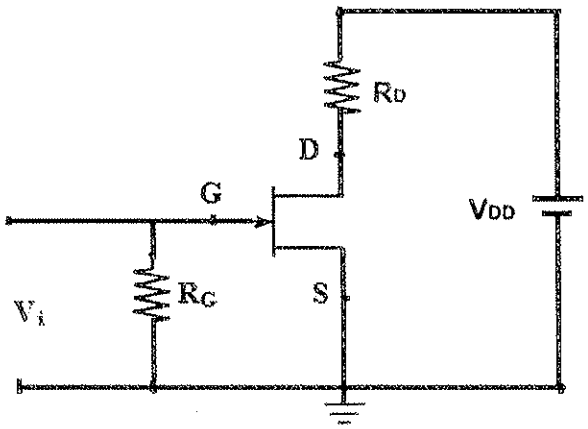


Fig. 16

Guide line 3: Replace DC source (V_{DD}) with short circuit.

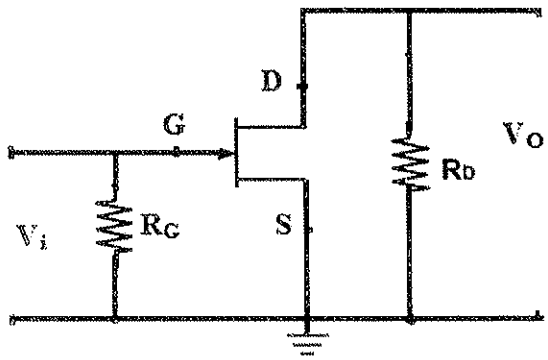


Fig. 17

Guide line 4: Replace FET terminals Gate (G), Drain (D) and Source (S) with its equivalent circuit.

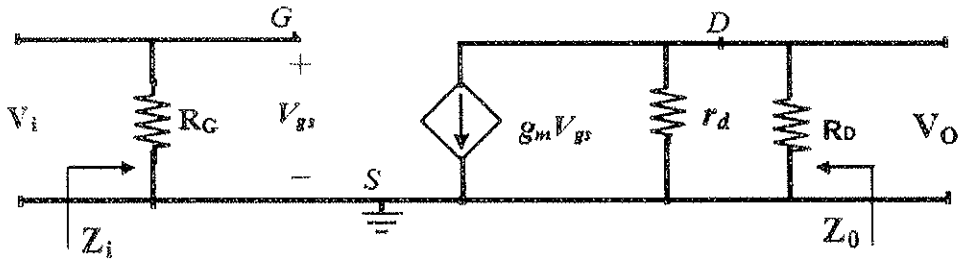


Fig. 18

Note that the ac equivalent circuit of Fig.18 is exactly the same as that of JFET amplifier using fixed bias configuration, shown in Fig. 10. Hence the results derived in section 4.5 for Z_i, Z_O & A_V can be readily applied to this circuit. Let us rewrite the results for reference.

- **Input Impedance (Z_i):**

$$Z_i = R_G$$

- **Output Impedance (Z_o):**

$$Z_o = r_d \,||\, R_D$$

$$Z_O = \frac{R_D r_d}{R_D + r_d}$$

If $r_d \geq 10R_D$,

$$Z_O \approx R_D$$

- **Voltage gain (A_V):**

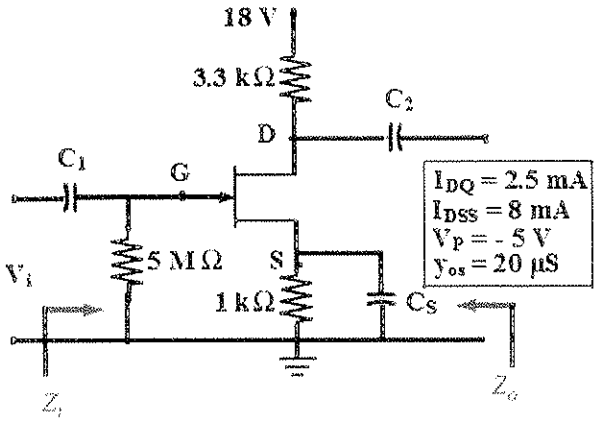
$$A_V = -\, g_m\,(r_d \,||\, R_D)$$

If $r_d \geq 10\, R_D$

$$A_V = -\, g_m\, R_D$$

Example 4.7 *For the FET amplifier shown below:* ***(a)*** *Calculate* Z_i, Z_o and A_V. ***(b)*** *Calculate* V_O if V_i = 10 mV (p-p). ***(c)*** *Calculate* Z_i, Z_o, and A_V *by ignoring the effect of* r_d.

Solution:



Given :

$I_{DQ} = 2.5$ mA	$R_G = 5$ MΩ
$I_{DSS} = 8$ mA	$R_D = 3.3$ kΩ
$V_P = -5$ V	$R_S = 1$ kΩ
$y_{os} = 20$ μS	$V_{DD} = 18$ V

For Self bias circuit, We know that:

$V_{GS} = -I_D R_S = -(2.5\times10^{-3}\times1\times10^{3})$

$V_{GS} = -2.5$ V

a)

- $g_{m0} = \dfrac{2I_{DSS}}{|V_P|}$

$= \dfrac{2\times8\times10^{-3}}{5}$

$g_{m0} = 3.2$ mS

- $g_m = g_{mo}\left(1 - \dfrac{V_{GS}}{V_P}\right)$

$= (3.2\times10^{-3})\left(1 - \dfrac{-2.5}{-5}\right)$

$g_m = 1.6$ mS

- **$r_d = \dfrac{1}{Y_{OS}} = (1/20\times10^{-6}) = 50$ kΩ**
- **$Z_i = R_G = 5$ MΩ**
- $Z_O = (r_d \,||\, R_D) = \dfrac{R_D r_d}{R_D + r_d}$

$= \dfrac{(50\times10^{3})(3.3\times10^{3})}{(50\times10^{3})+(3.3\times10^{3})}$

- **$Z_O = 3.09$ kΩ**
- $A_V = -g_m (r_d \,||\, R_D)$

$= -(1.6\times10^{-3})(3.09\times10^{3})$

$A_V = -4.944$

b)

We know that,

- $A_V = \dfrac{V_O}{V_i}$

Therefore,

- $V_o = A_V V_i$

$= -(4.944\times10\times10^{-3})$

- **$V_o = -49.44$ mV (p-p)**

c)

When r_d is neglected:

- **$Z_i = R_G = 5$ MΩ**
- **$Z_O = R_D = 3.3$ kΩ**
- $A_V = -g_m R_D$

$= -(1.6\times10^{-3})(3.3\times10^{3})$

$A_V = -5.28$

Example 4.8 *The self-bias configuration has an operating defined by* $V_{GSQ} = -2.6$ V & $I_{DQ} = 2.6$ mA, with $I_{DSS} = 8$ mA, $V_P = -6$V, $R_D = 3.3$ kΩ, $R_G = 1$ MΩ, $R_S = 1$ kΩ, $V_{DD} = 20$ V and $y_{os} = 25$ μS. ***(a)*** *Determine* Z_i, Z_o and A_V. ***(b)*** *Determine* Z_i, Z_o, and A_V *without the effect of* r_d.

Solution:

Given : $V_P = -6$ V, $R_G = 1$ MΩ, $V_{DD} = 20$ V, $I_{DQ} = 2.6$ mA, $y_{os} = 25$ μS, $R_D = 3.3$ kΩ, $V_{GSQ} = -2.6$ V, $I_{DSS} = 8$ mA, $R_S = 1$ kΩ

a)

- $g_{m0} = \frac{2I_{DSS}}{|V_P|}$

$= \frac{2\times8\times10^{-3}}{56}$

$g_{m0} = 2.67$ mS

- $g_m = g_{m0}(1 - \frac{V_{GS}}{V_P})$

$= (2.67\times10^{-3})(1 - \frac{-2.6}{-6})$

$g_m = 1.51$ mS

- $r_d = \frac{1}{Y_{OS}} = (1/25\times10^{-6}) = 40$ kΩ

- $Z_i = R_G = 1$ MΩ

- $Z_0 = (r_d \,||\, R_D) = \frac{R_D r_d}{R_D + r_d}$

$= \frac{(40\times10^3)(3.3\times10^3)}{(40\times10^3)+(3.3\times10^3)}$

- $Z_0 = 3.05$ kΩ

- $A_V = -g_m(r_d \,||\, R_D)$

$= -(1.51\times10^{-3})(3.05\times10^3)$

$A_V = -4.6055$

b)

When r_d is neglected:

- $Z_i = R_G = 1$ MΩ
- $Z_O = R_D = 3.3$ kΩ
- $A_V = -g_m R_D$

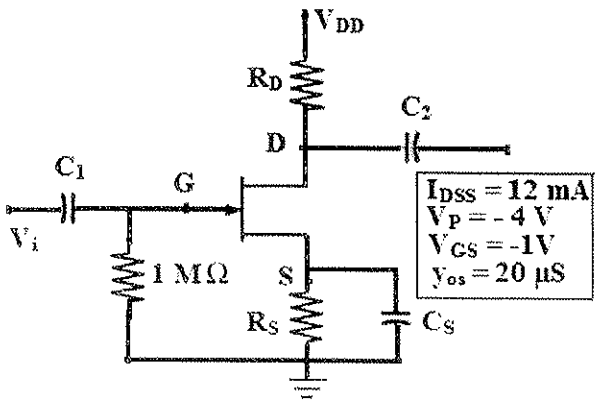
$= -(1.51\times10^{-3})(3.3\times10^3)$

$A_V = -4.983$

Example 4.9 *Determine the value of* R_D *for the circuit of figure below that will result in a gain of -10.*

Solution:

Given : $I_{DSS} = 12$ mA, $V_P = -4$ V, $A_V = -10$, $R_G = 1$ MΩ, $V_{GS} = -1$V, $y_{os} = 20$ μS



- $g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2\times12\times10^{-3}}{4}$

$g_{m0} = 6$ mS

- $g_m = g_{m0}(1 - \frac{V_{GS}}{V_P})$

$= (6\times10^{-3})(1 - \frac{-1}{-4})$

$g_m = 4.5$ mS

- $r_d = \frac{1}{Y_{OS}} = (1/20\times10^{-6}) = 50$ kΩ

- $A_V = -g_m(r_d \,||\, R_D)$

$-10 = -(4.5\times10^{-3})(r_d \,||\, R_D)$

- $(r_d \,||\, R_D) = 2.23$ kΩ

- $(r_d \,||\, R_D) = \frac{R_D r_d}{R_D + r_d}$

$2.23\times10^3 = \frac{R_D(50\times10^3)}{R_D+(50\times10^3)}$

Therefore,

- $R_D = 2.34$ kΩ

4.7 JFET Common Source Amplifier Using Voltage Divider bias Configuration (with bypassed R_S) :

- The Voltage divider CS amplifier with input voltage Vi applied through coupling capacitor C_1 and connected to output through another coupling capacitor C_2 is shown in Fig. 19.
- The analysis of JFET CS amplifier for its small signal behavior can be made by following simple guidelines:

Guide line 1: Draw the actual circuit diagram.

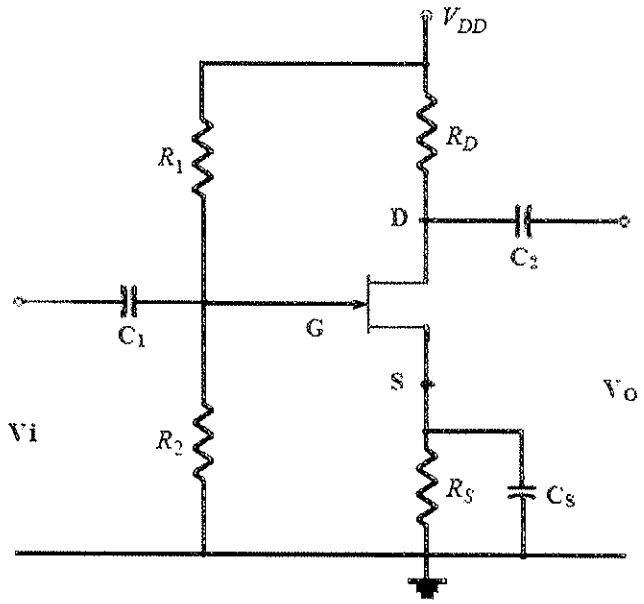


Fig. 19

Guide line 2: Replace Coupling capacitors and bypass capacitor with short circuit. (Because the capacitors are selected in such a way that they should offer very less reactance to the AC)

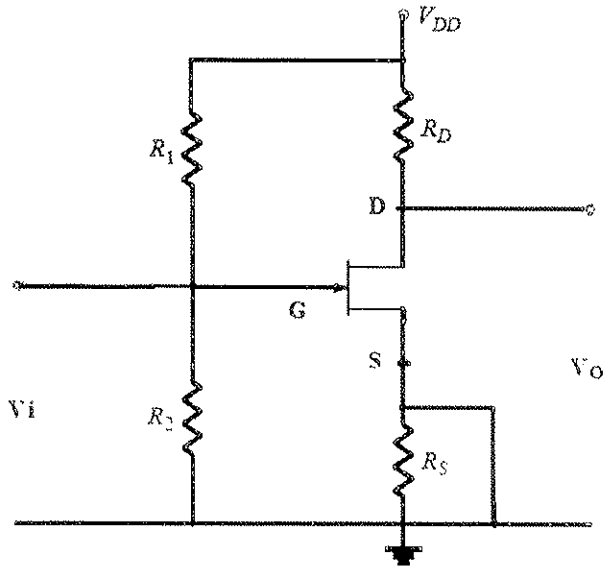


Fig. 20

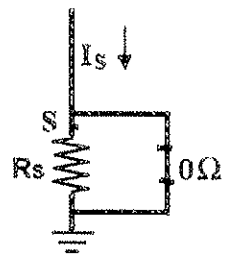


Fig. 21

From the Fig. 21 it is observed that, after short circuiting coupling capacitor CS, the resistance R_S is in parallel with zero ohms. So their parallel combination is also zero. Therefore, resistance R_S in Fig. 20 can be replaced with 0 Ω.

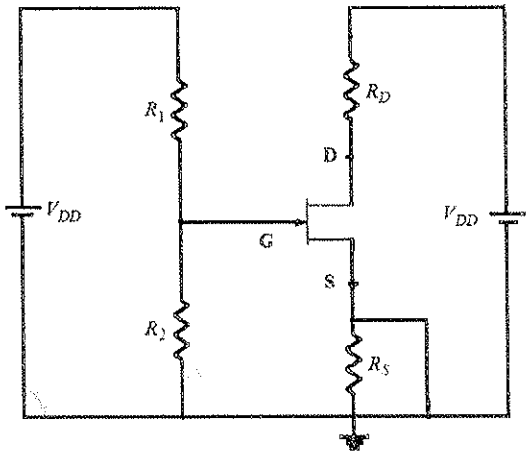


Fig.22

Guide line 3: Replace DC source (V_{DD}) with short circuit.

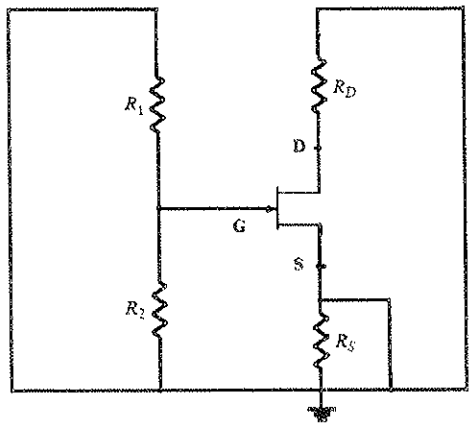


Fig. 23

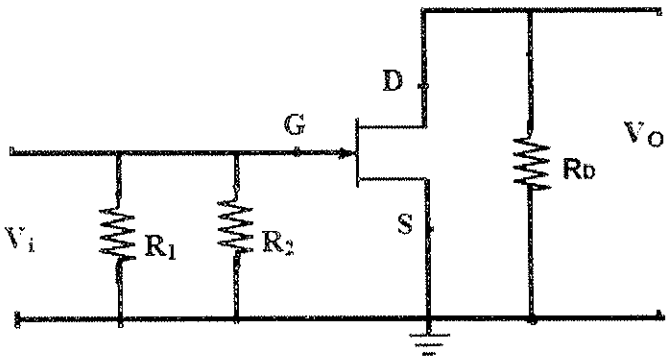


Fig. 24

Guide line 4: Replace FET terminals Gate (G), Drain (D) and Source (S) with its equivalent circuit.

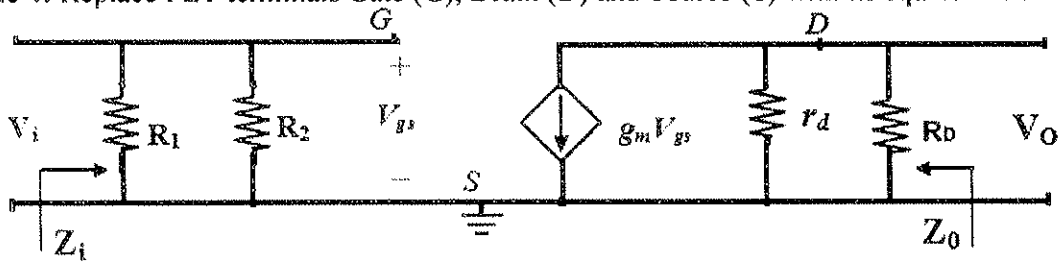


Fig. 25

Note that the ac equivalent circuit of Fig. 25 is exactly the same as that of JFET amplifier using fixed bias configuration, shown in Fig. 10. Hence the results derived in section 4.5 for Z_i, Z_O & A_V can be readily applied to this circuit. The only exception is that, R_G should be replaced by $R_1 \,||\, R_2$. Let us rewrite the results for reference.

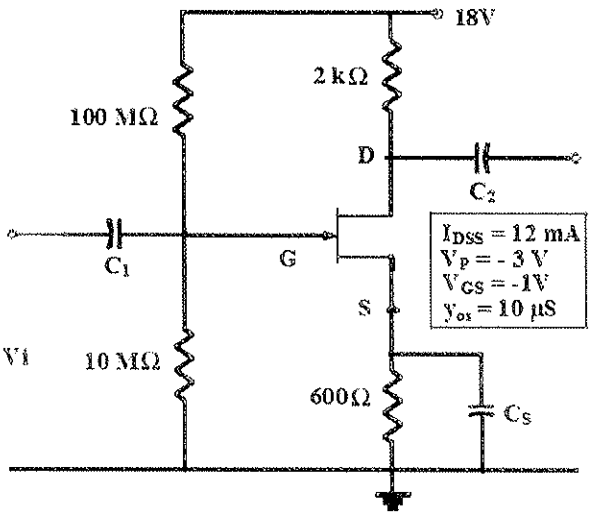
- **Input Impedance (Z_i):** $Z_i = (R_1 \,||\, R_2)$
- **Output Impedance (Z_0):** $Z_0 = (r_d \,||\, R_D)$

  If $r_d \geq 10R_D$, $Z_0 \approx R_D$
- **Voltage gain (A_V):** $A_V = -g_m (r_d \,||\, R_D)$

  If $r_d \geq 10\ R_D$ $A_V = -g_m R_D$

Example 4.10 *For the JFET amplifier shown below: (a) Calculate* Z_i, Z_O and A_V. *(b) Find* V_O *if* $V_i = 25\ mV$.

Solution:



Given :
$I_{DSS} = 12$ mA
$V_P = -3$ V
$V_{GS} = -1$V
$V_{DD} = 18$V
$R_1 = 100$ MΩ
$R_2 = 10$ MΩ
$R_D = 2$ kΩ
$R_S = 600$ Ω
$y_{os} = 10$ μS

- $g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2\times12\times10^{-3}}{3}$
  $g_{m0} = 8$ mS
- $g_m = g_{mo}(1 - \frac{V_{GS}}{V_P})$
  $= (8\times10^{-3})(1 - \frac{-1}{-3})$
  $g_m = 5.33$ mS
- **$r_d = \frac{1}{Y_{OS}} = (1/10\times10^{-6}) = 100$ kΩ**
- $Z_i = (R_1 \,||\, R_2)$
  $Z_i = (100\ M\Omega \,||\, 10\ M\Omega)$
  $Z_i = 9.09\ M\Omega$
- $Z_O = (r_d \,||\, R_D)$
  $Z_O = (100\ k\Omega \,||\, 2\ k\Omega)$
  $Z_O = 1.96\ k\Omega$
- $A_V = -g_m (r_d \,||\, R_D)$
  $= -(5.33\times10^{-3})(1.95\times10^{3})$
- **$A_V = -10.44$**

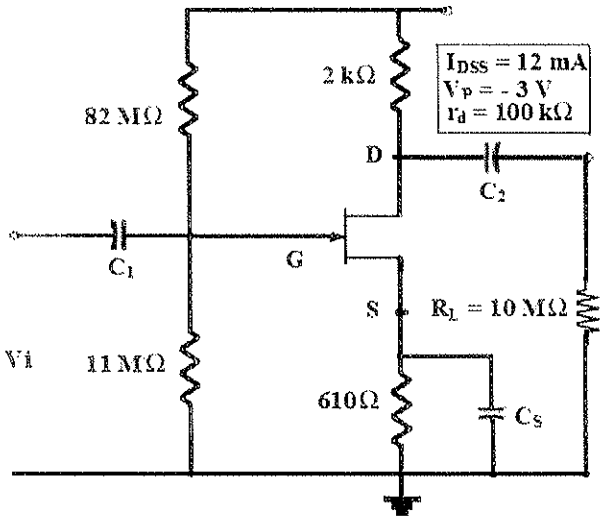
We know that,

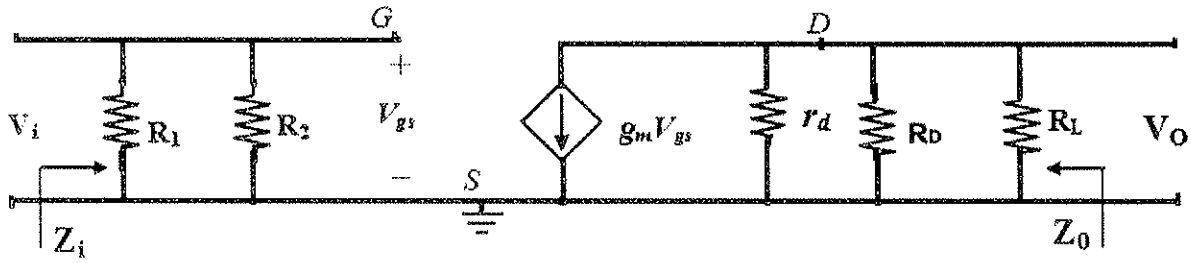
- $A_v = \frac{V_O}{V_i}$ Therefore,
- $V_o = A_V V_i$
  $= -(10.44\times25\times10^{-3})$
- **$V_o = -0.261$ V**

Example 4.11 *Determine* Z_i, Z_O and V_O *for the network shown below: if* $V_i = 20$ *mV and* $V_{GSQ} = -0.95$ *V.*

Solution:

Given :
$I_{DSS} = 12$ mA
$V_P = -3$ V
$V_{GS} = -0.95$ V
$V_i = 20$ mV
$R_L = 10$ MΩ
$R_1 = 82$ MΩ
$R_2 = 11$ MΩ
$R_D = 2$ kΩ
$R_S = 610$ Ω
$r_d = 100$ kΩ





- $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2\times12\times10^{-3}}{3}$
  $\mathbf{g_{m0} = 8\ mS}$

- $g_m = g_{mo}\left(1 - \dfrac{V_{GS}}{V_P}\right)$
  $= (8\times10^{-3})\left(1 - \dfrac{-0.95}{-3}\right)$
  $\mathbf{g_m = 5.47\ mS}$

- $Z_i = (R_1 \,||\, R_2)$
  $Z_i = (11\ M\Omega \,||\, 82\ M\Omega)$
  $Z_i = 9.7\ M\Omega$

- $Z_O = (r_d \,||\, R_D \,||\, R_L)$
  $Z_O = (100\ k\Omega \,||\, 2\ k\Omega \,||\, 10\ M\Omega)$
  $Z_O = 1.97\ k\Omega$

- $A_V = -g_m (r_d \,||\, R_D \,||\, R_L)$
  $= -(5.47\times10^{-3})(1.97\times10^{3})$
- $\mathbf{A_V = -10.77}$

We know that,

- $A_v = \dfrac{V_O}{V_i}$ Therefore,
- $V_o = A_V V_i$
  $= -(10.77\times20\times10^{-3})$
- $\mathbf{V_o = -0.21538\ V}$
- $\mathbf{V_o = -215.38\ mV}$